

Fig 1

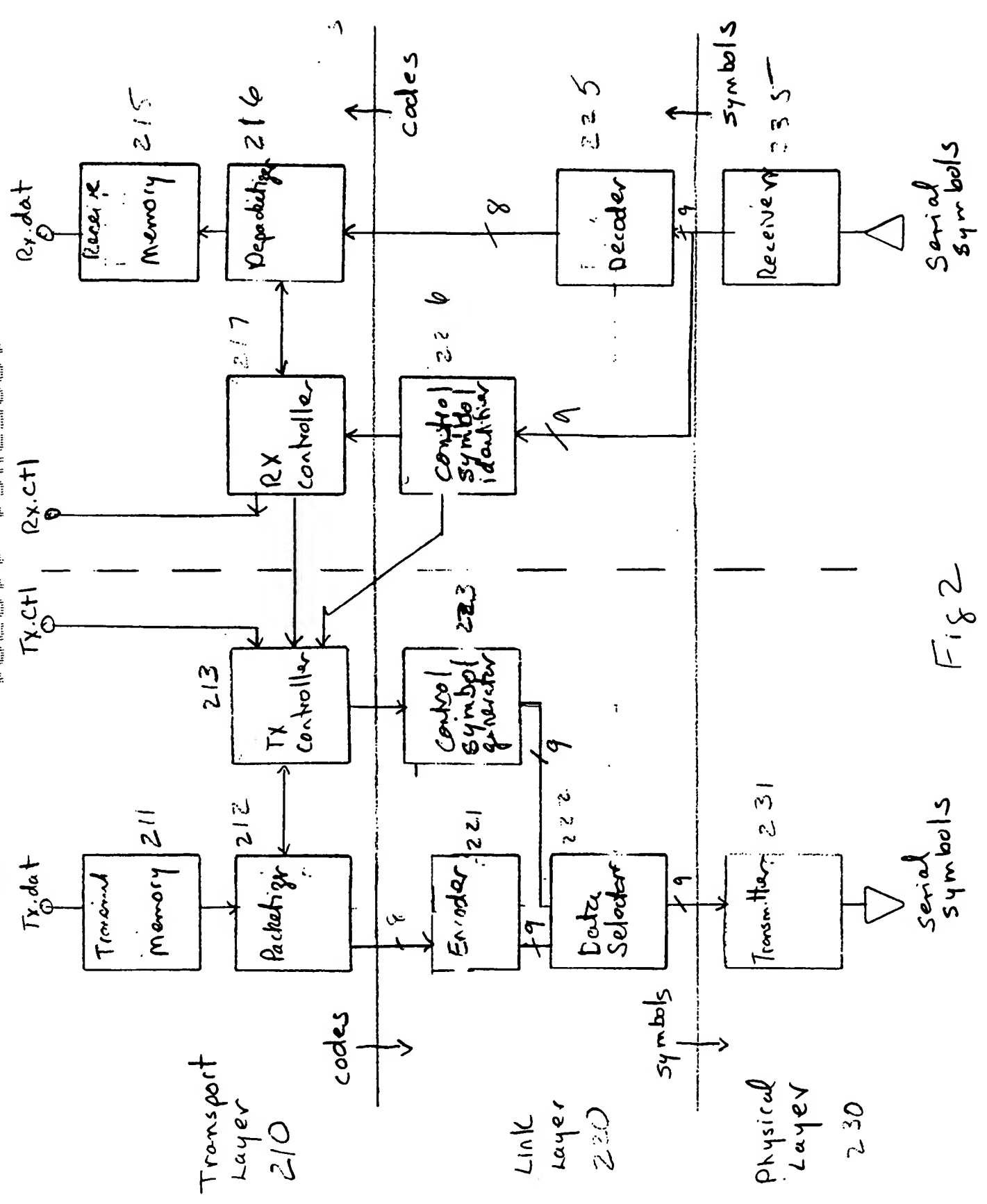


Fig 2

Physical Layer

230

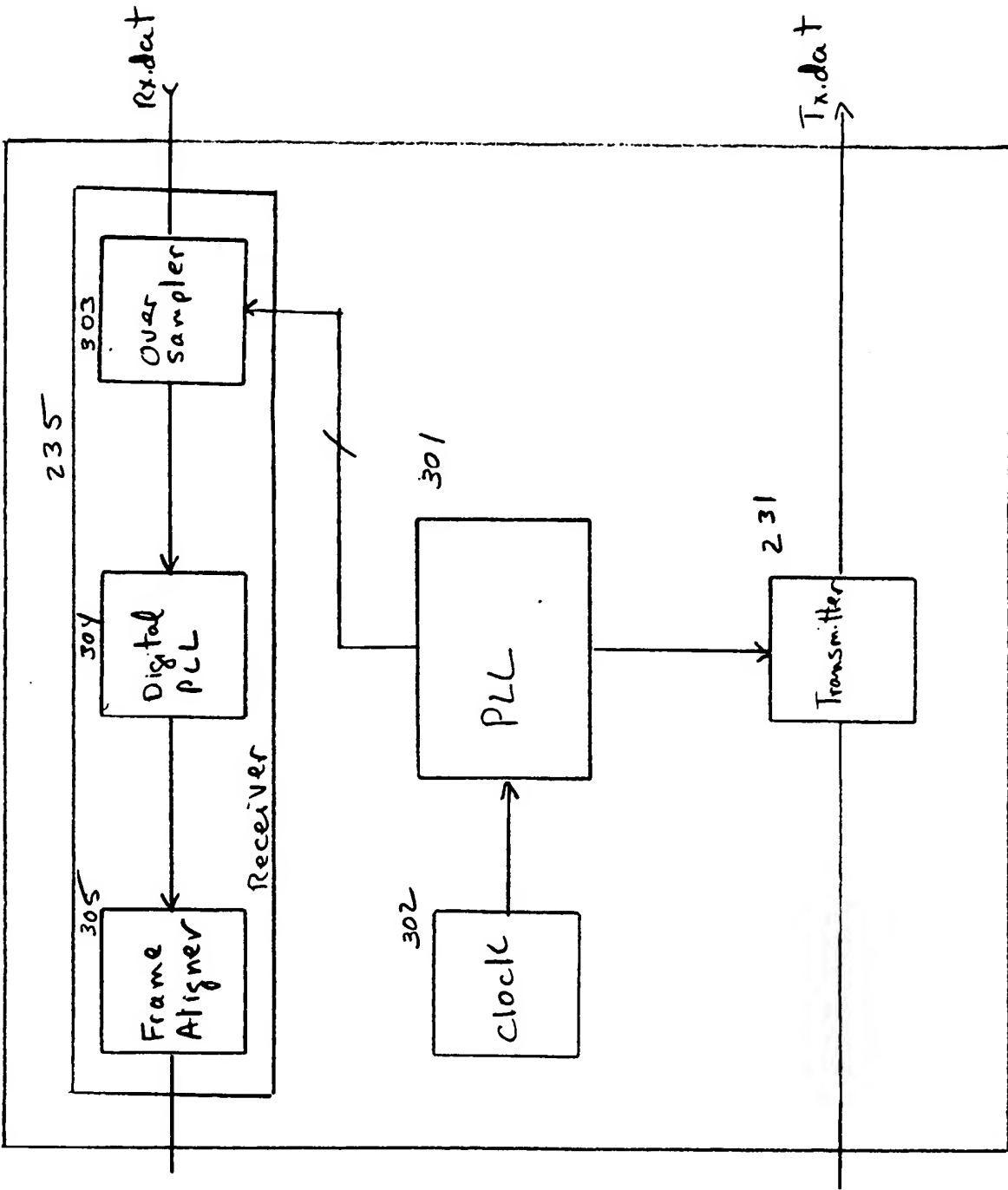


Fig 3

Packet

400

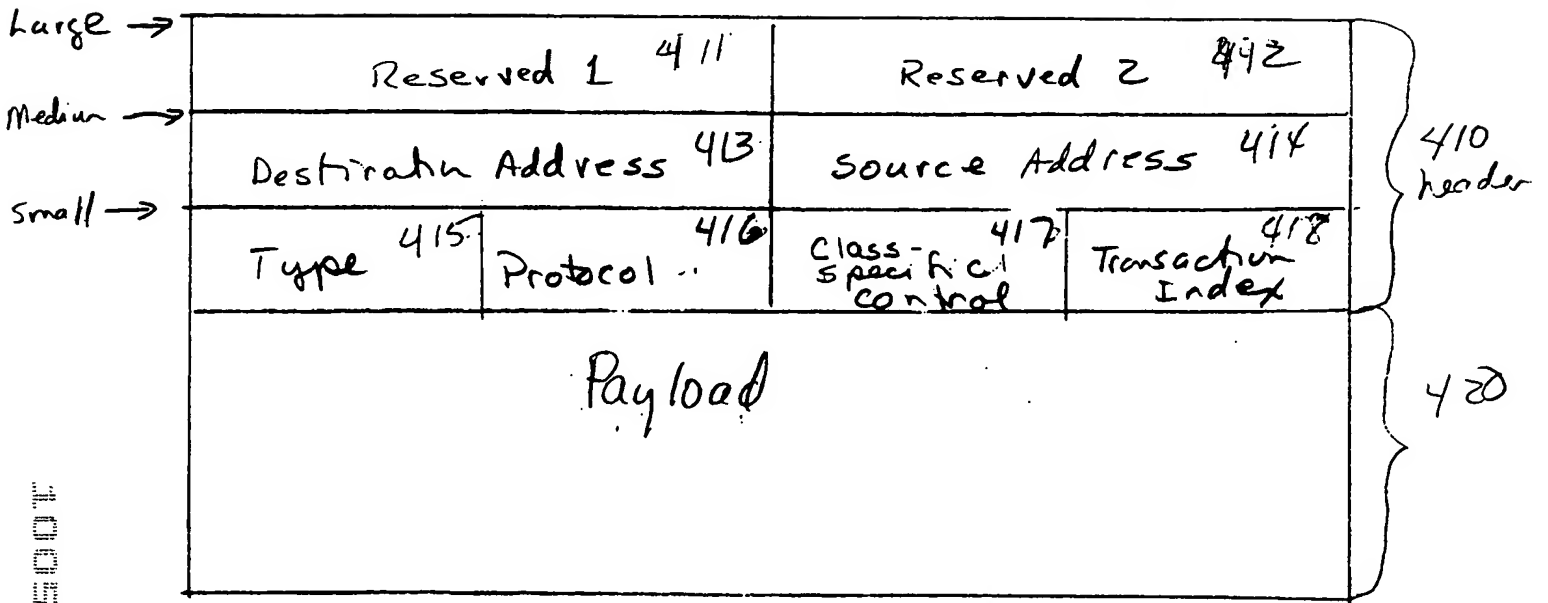
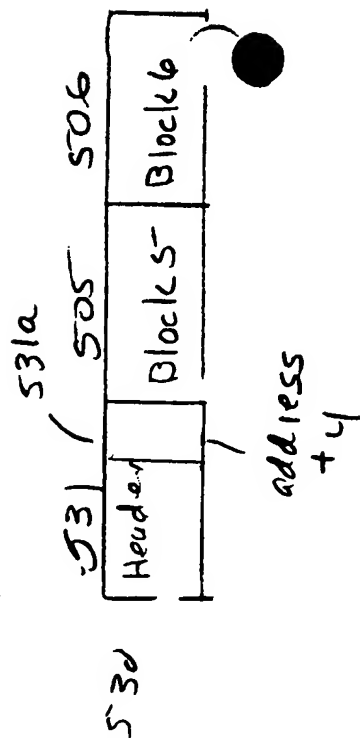
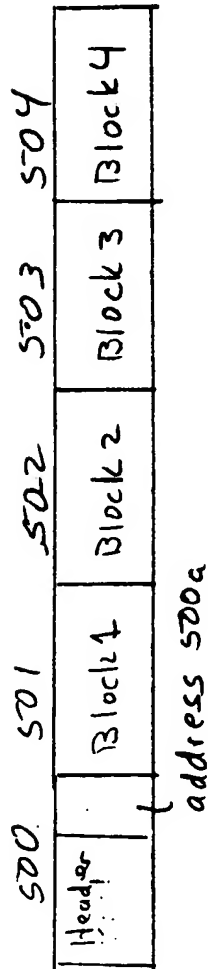
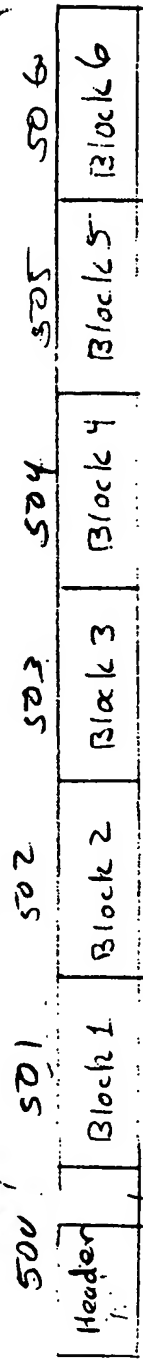


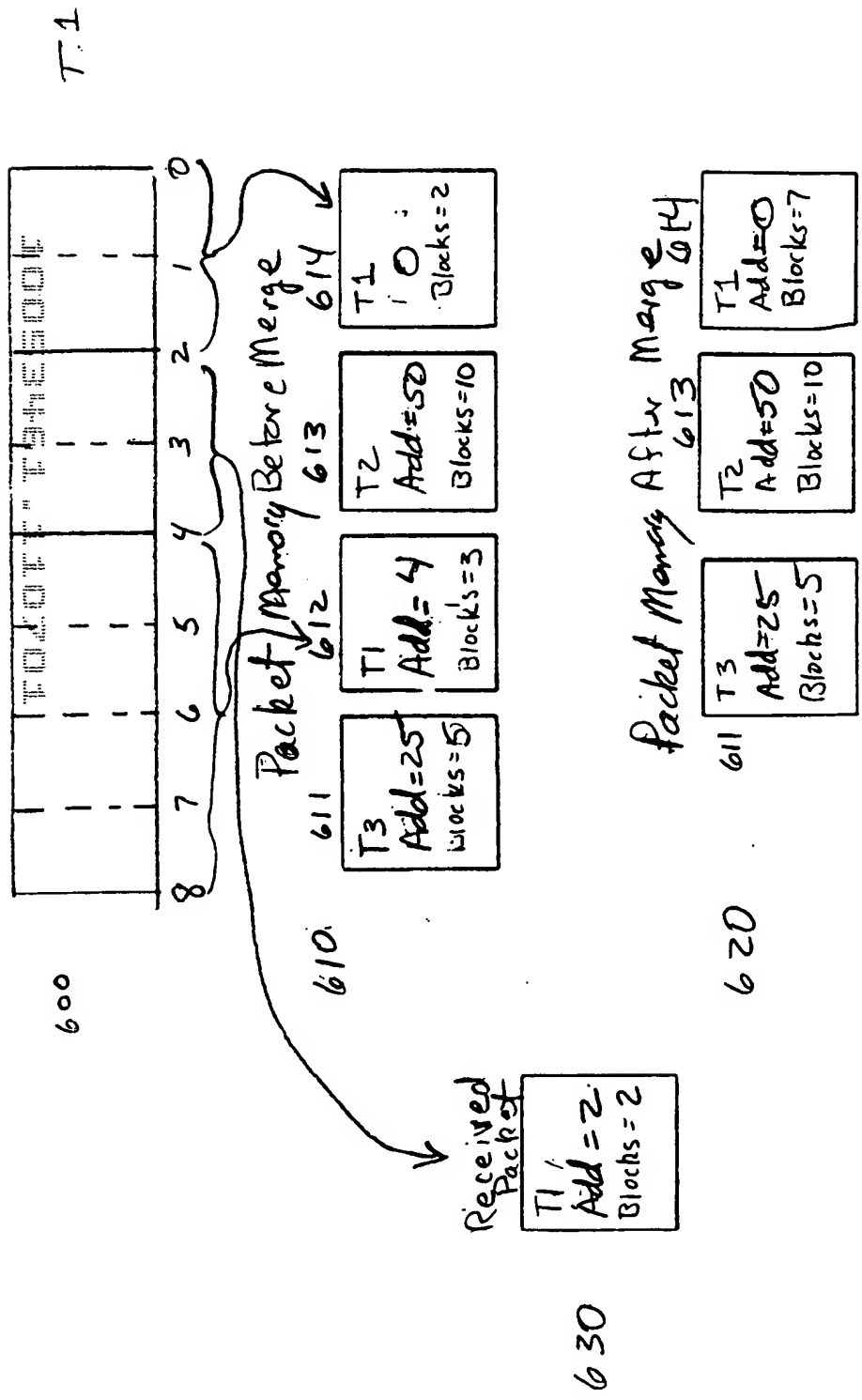
Fig 4

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for payload shift



F. 35



F. 86

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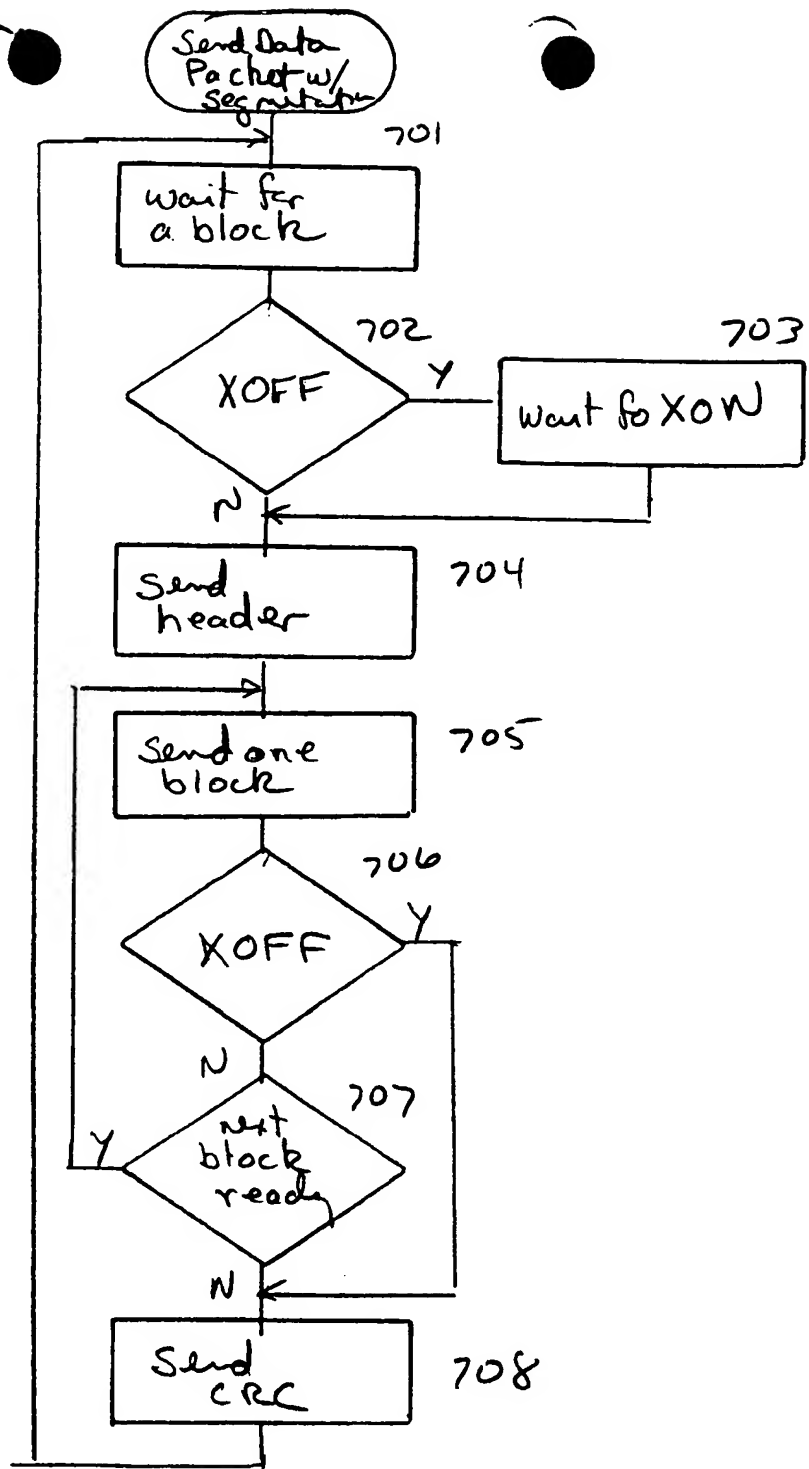


Fig 7

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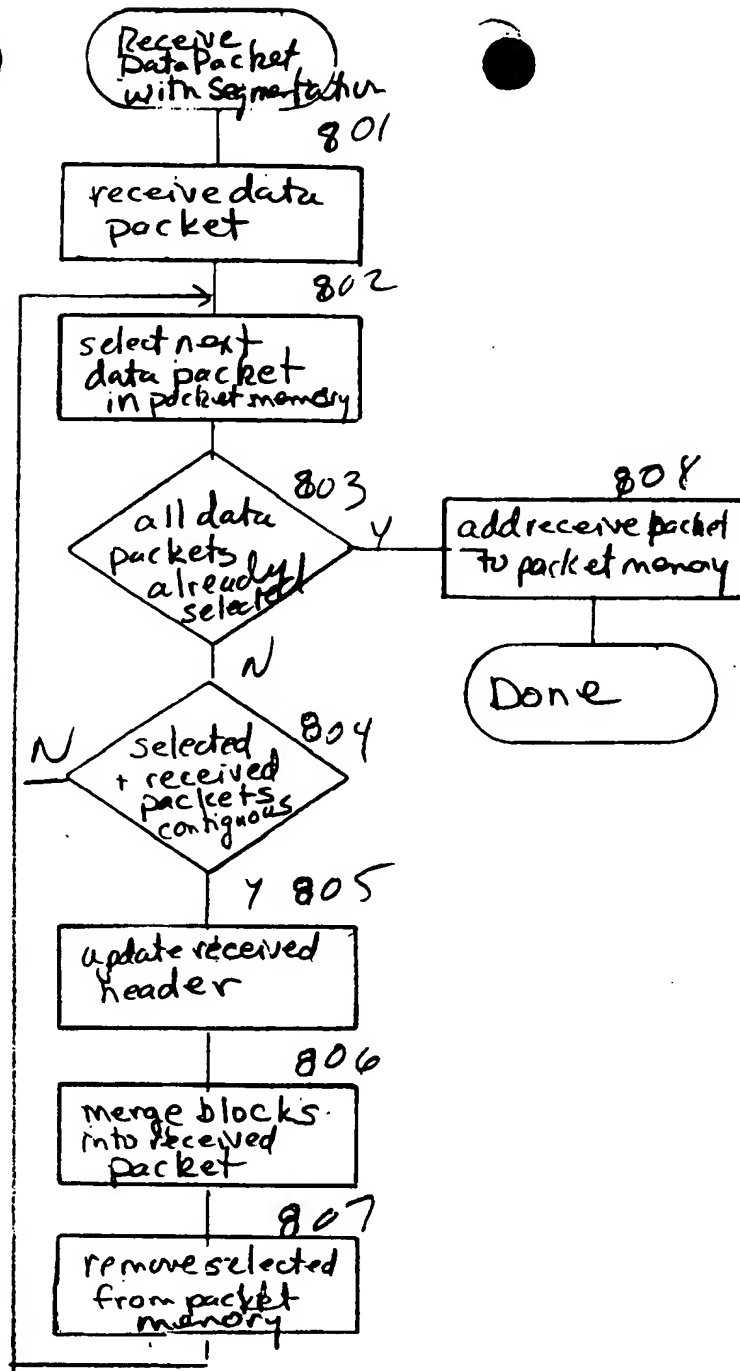
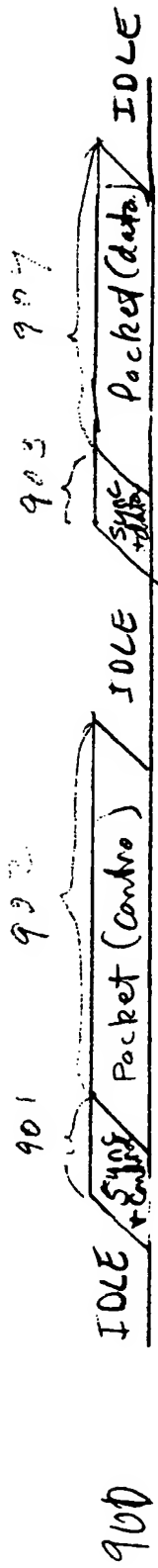


Fig 8



Sync + packet type

Fig 9A

BIT BUFFER	A8	A7	A6	A5	A4	A3	A2	A1	A0	B8	B7	B6	B5	B4	B3	B2	B1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0
BIT CONTENT	0	0	1	0	0	0	0	0	0	1	1	1	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0
"10" DETECTION	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
"10" DETECTION	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
RESULT	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Symbol																											
STARTING POINTS																											

FIG.10

Fig 9B

910

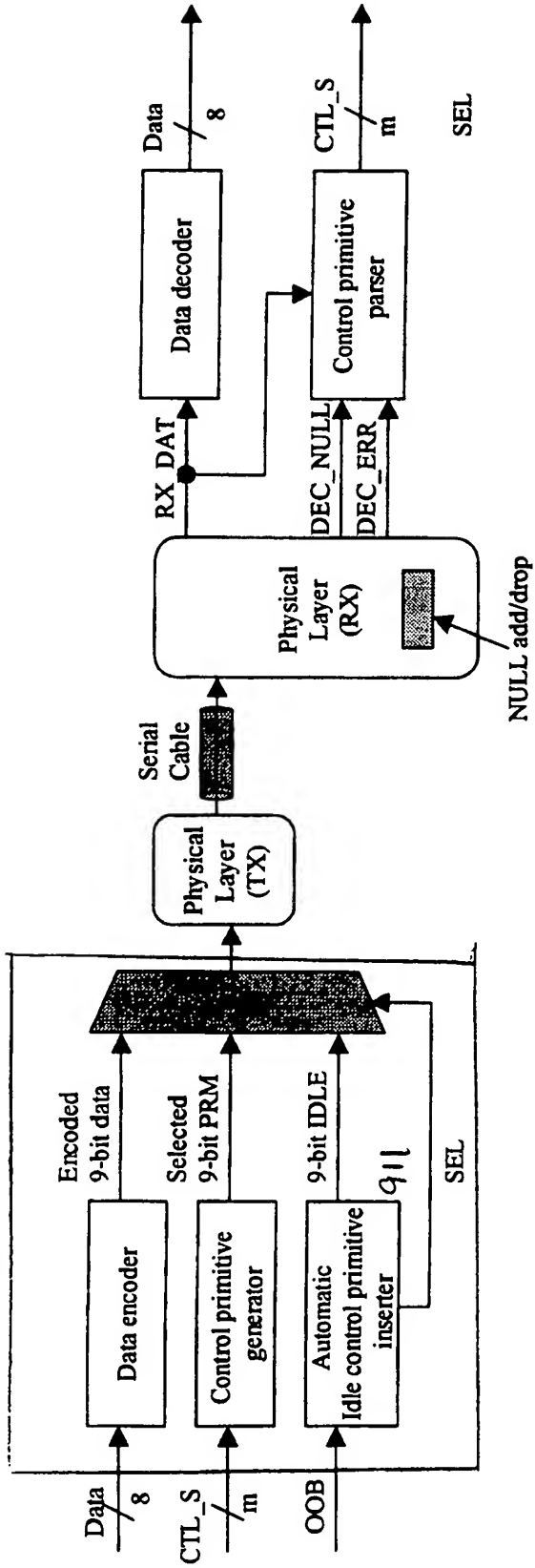


Fig. 9C

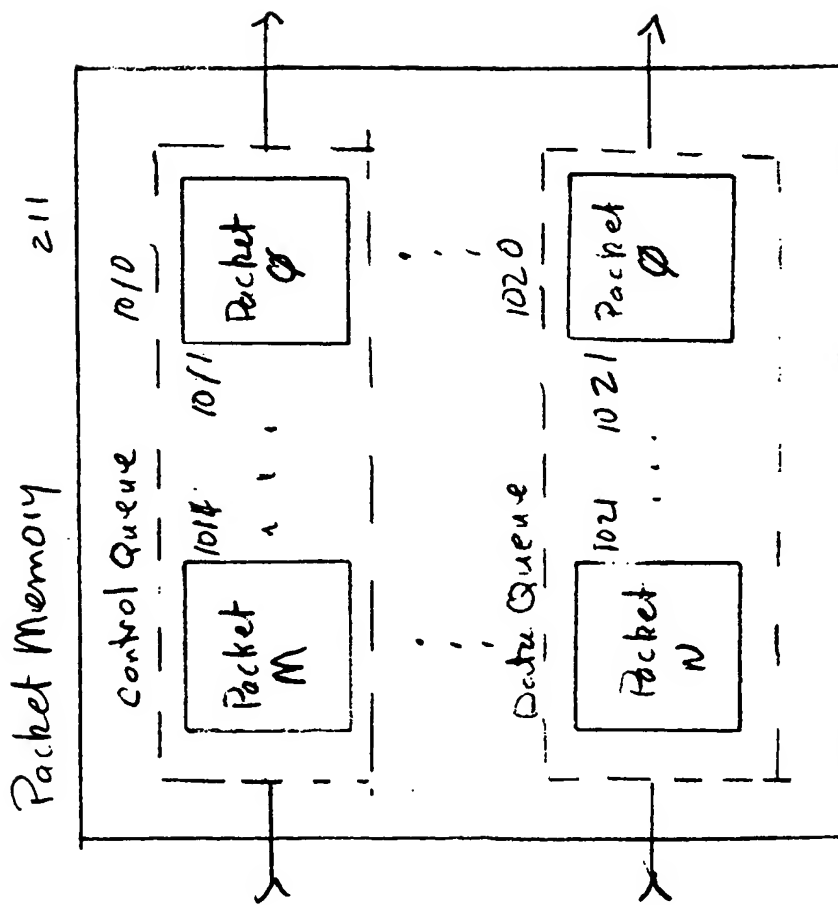


FIG. 10

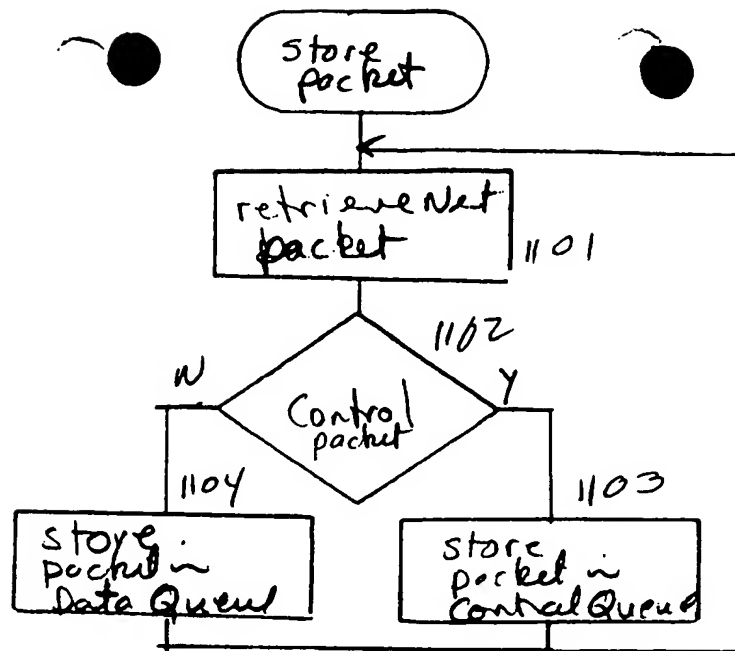


Fig 11

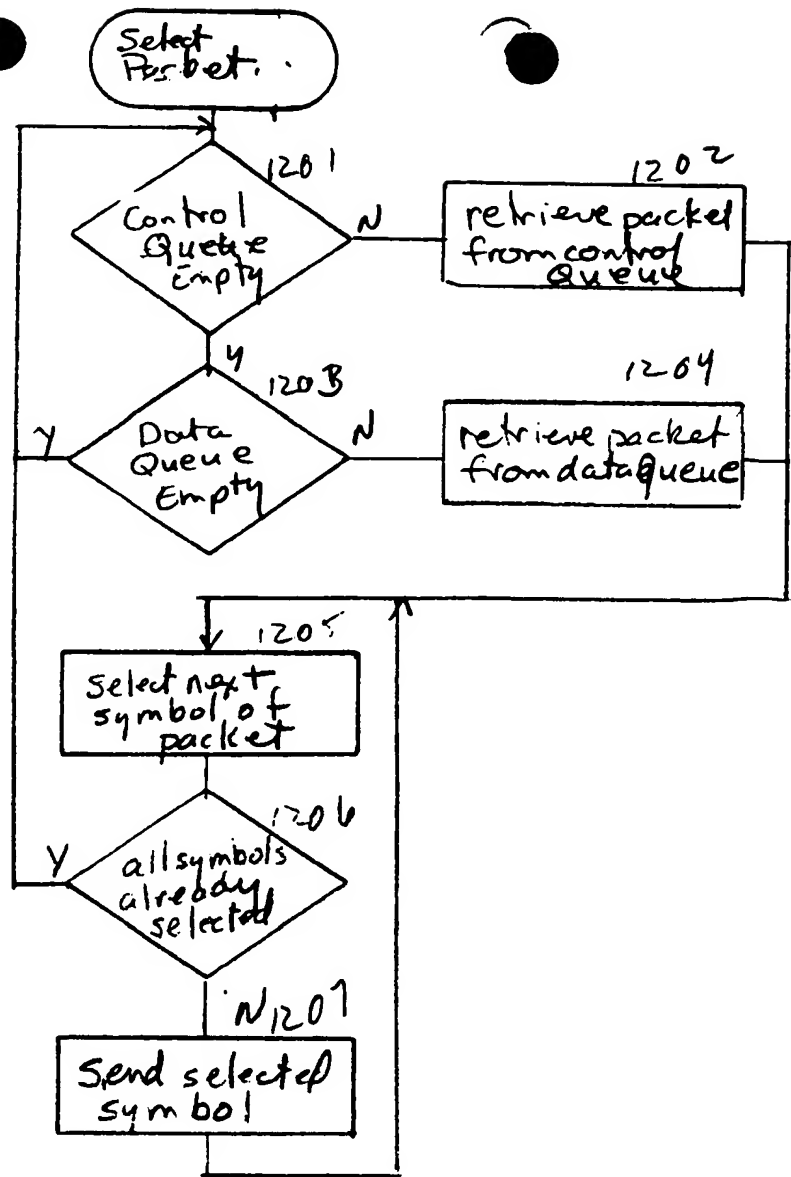


Fig 12



Fig 13

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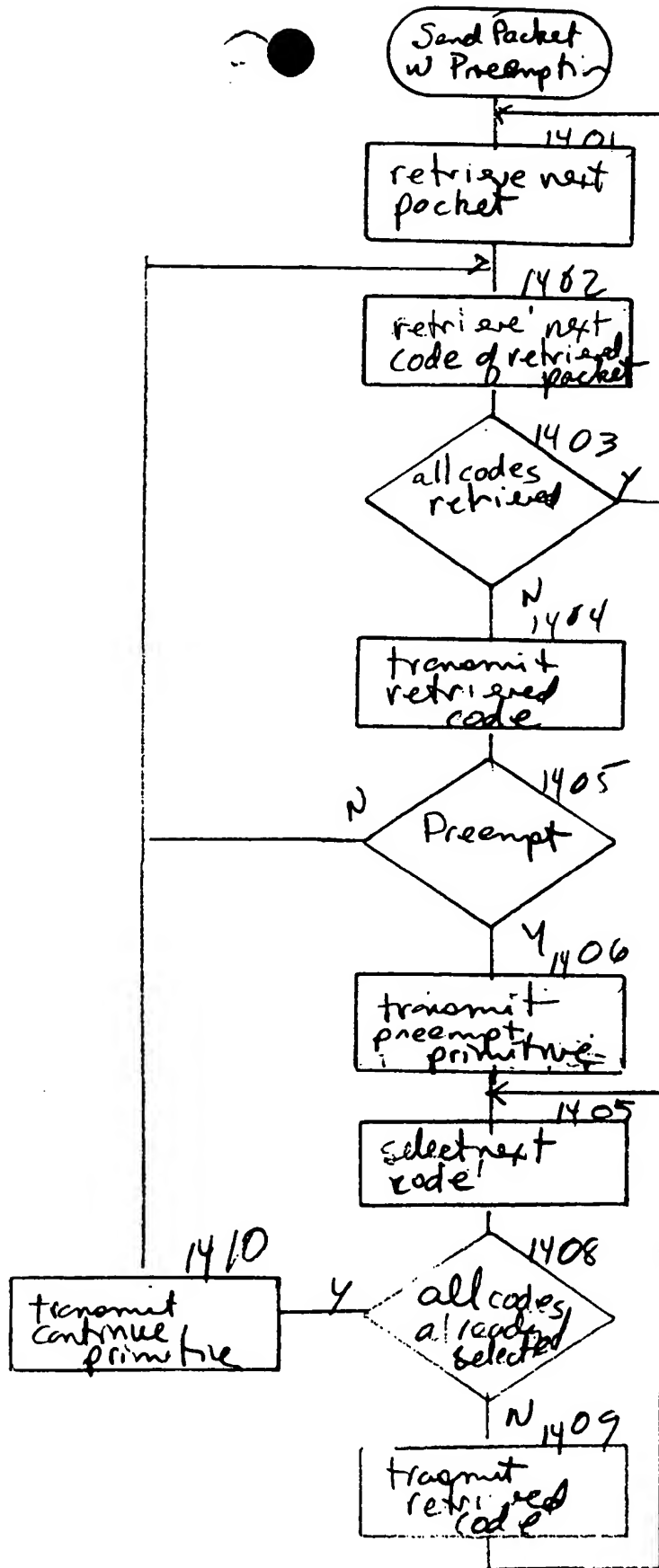


Fig 14

10053461.110701

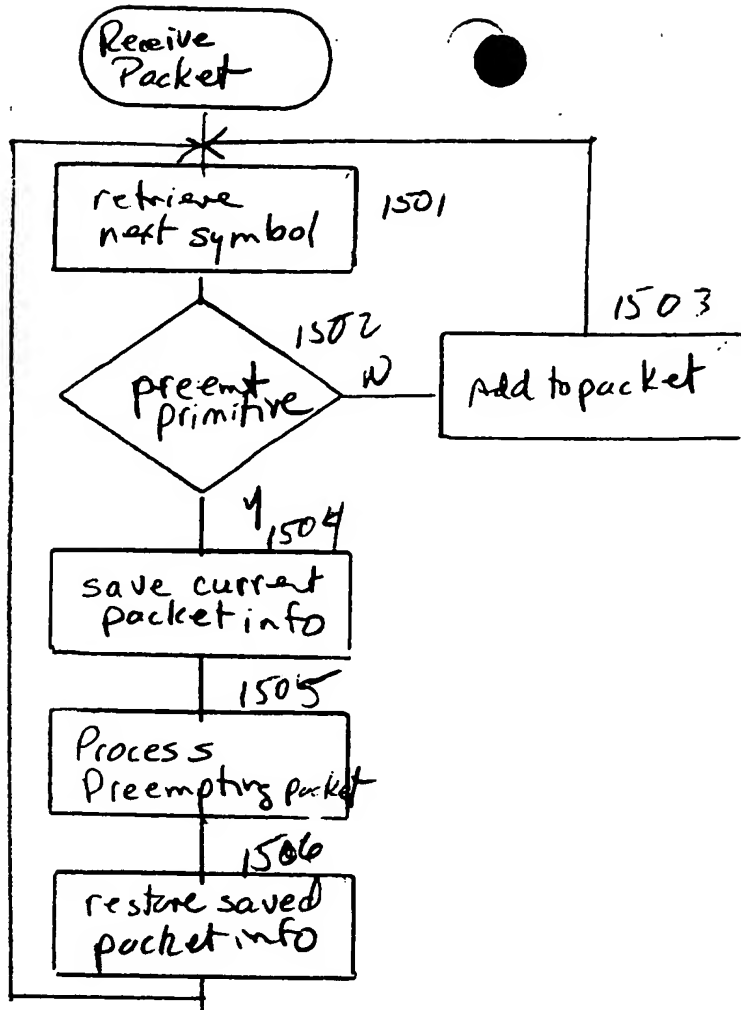


Fig 15

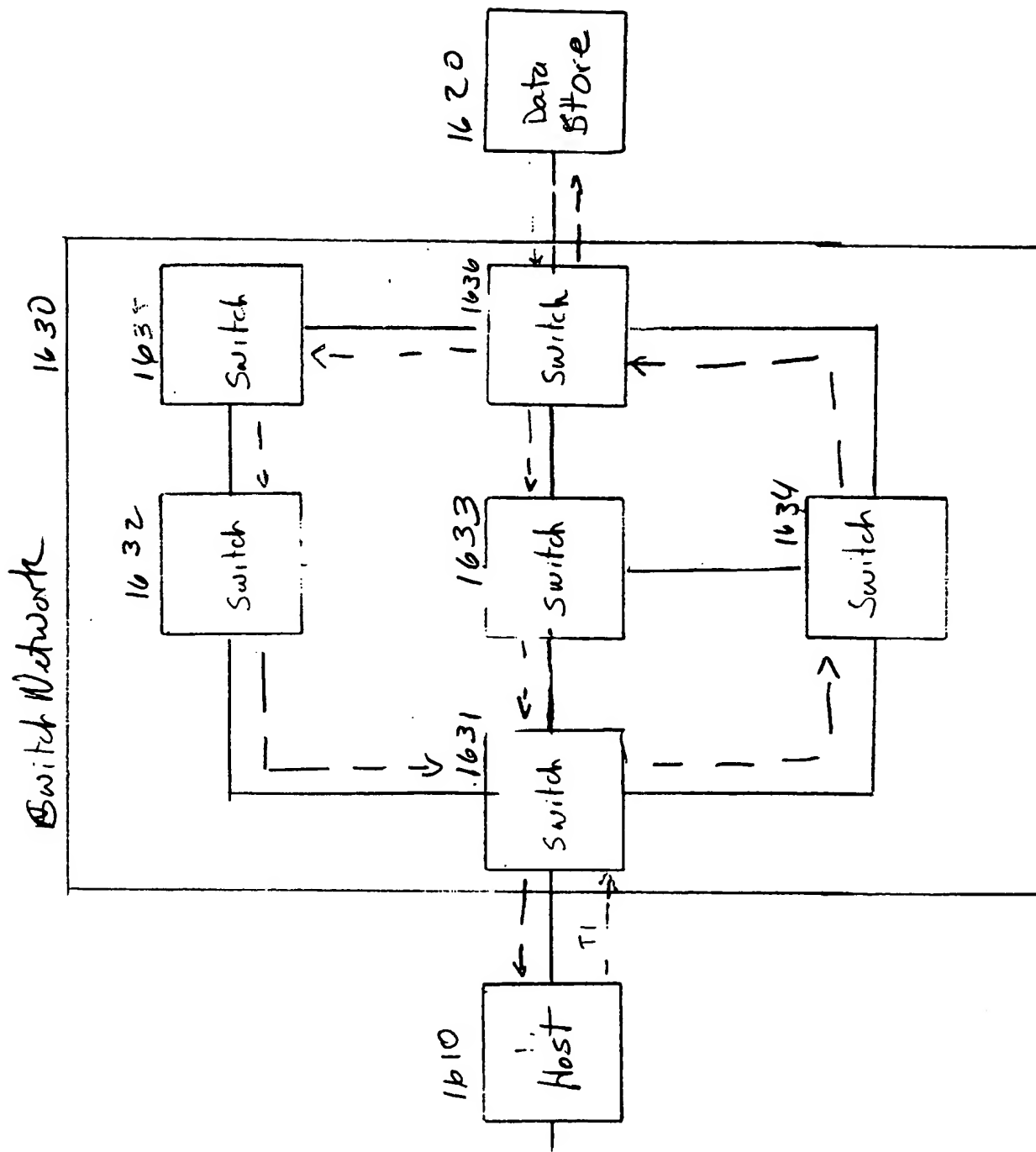
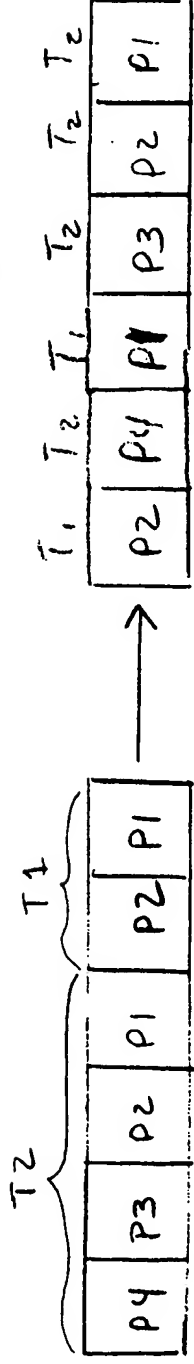


Fig 16

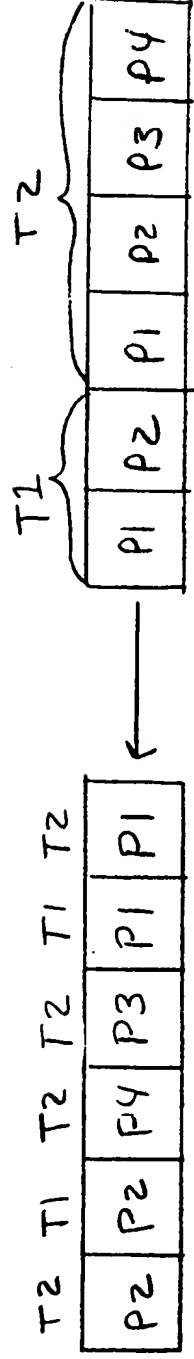
TOGETHER THE STORE

Host



1701

Preserving Packet Order w/ Transaction



1702

No Packet or Transaction Ordering

Fig 17

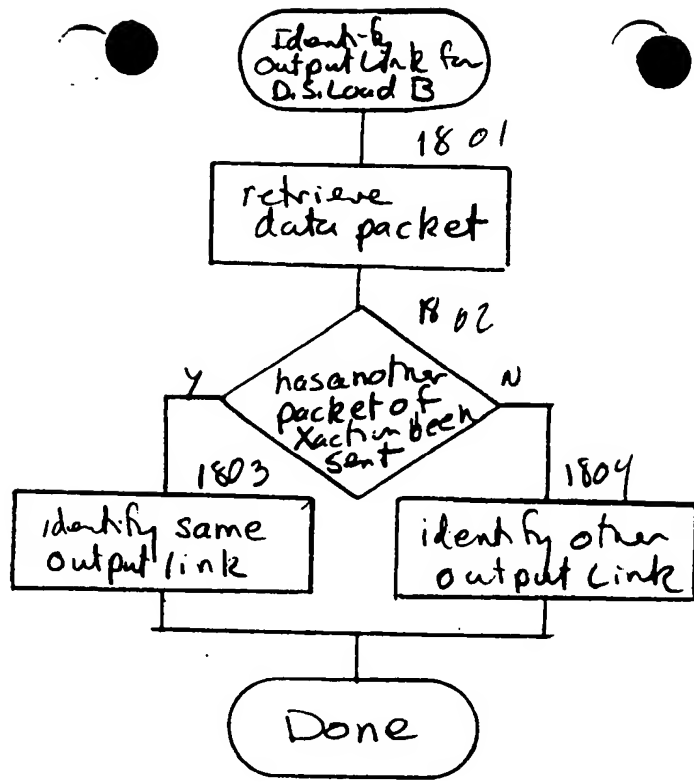


Fig 18

1053461-110701

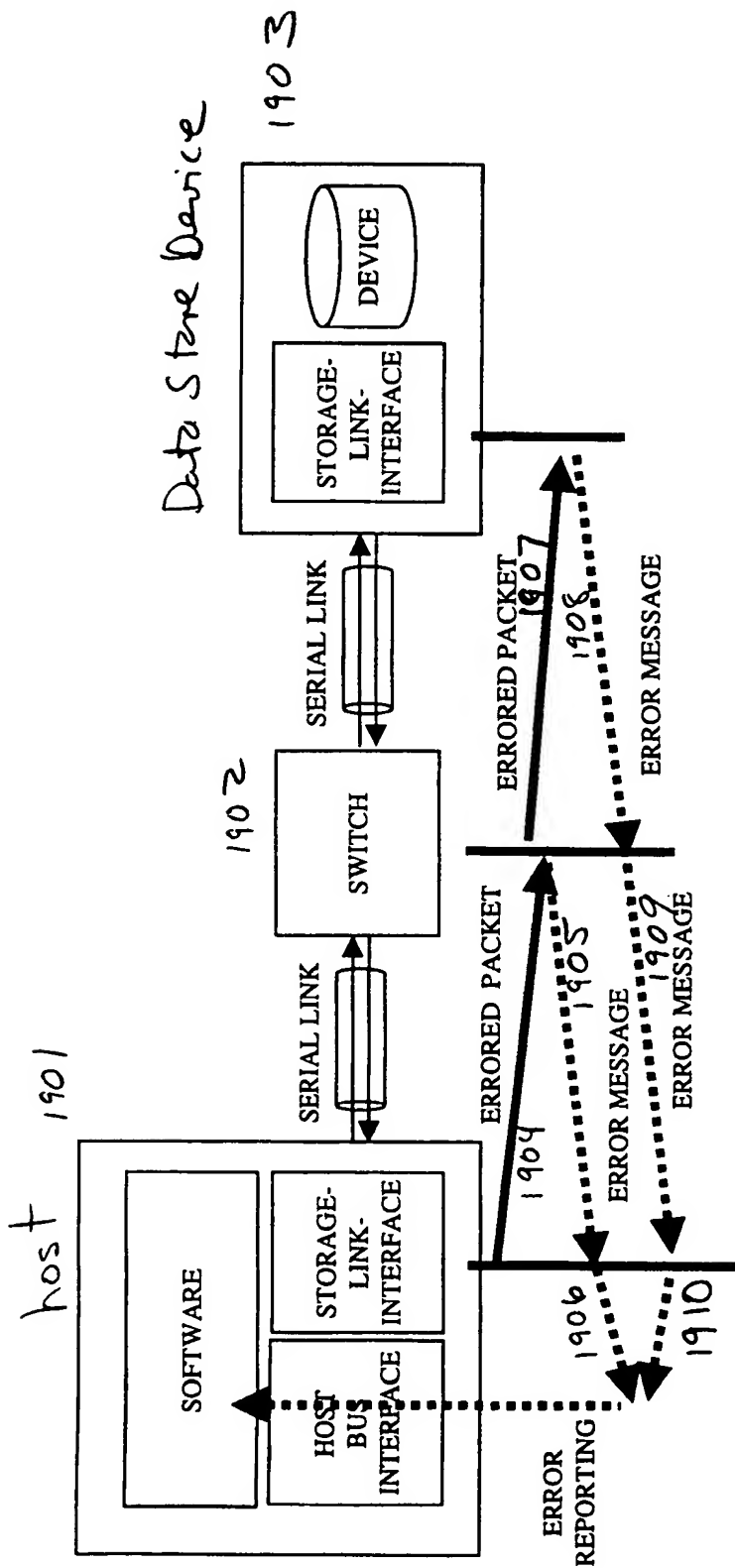


Fig 19A

1901A

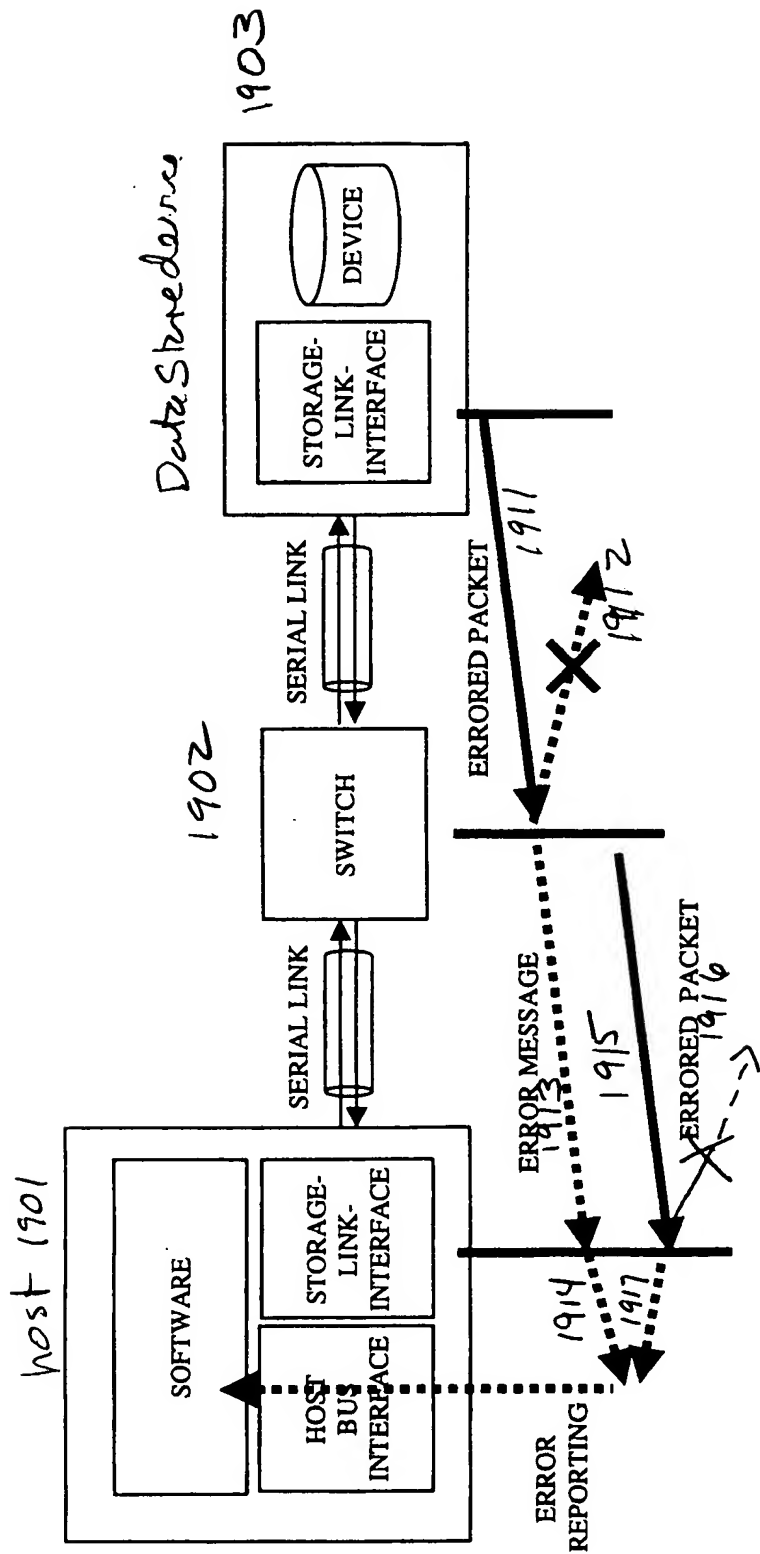
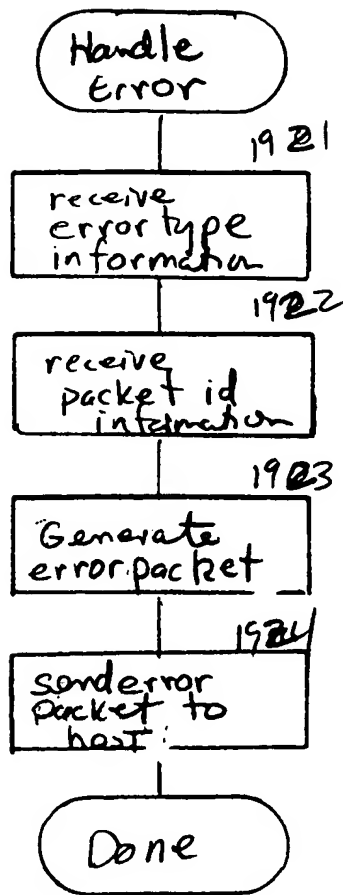


Fig 19B

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19C

8b Code	9 bit symbol
0000 0000	101010101
0000 0001	101010100
0000 0010	101010111
⋮	
0101 0101	001010101
⋮	
0111 0110	001110110
0111 0111	100100010
⋮	
1111 1111	110101010

Fig 20

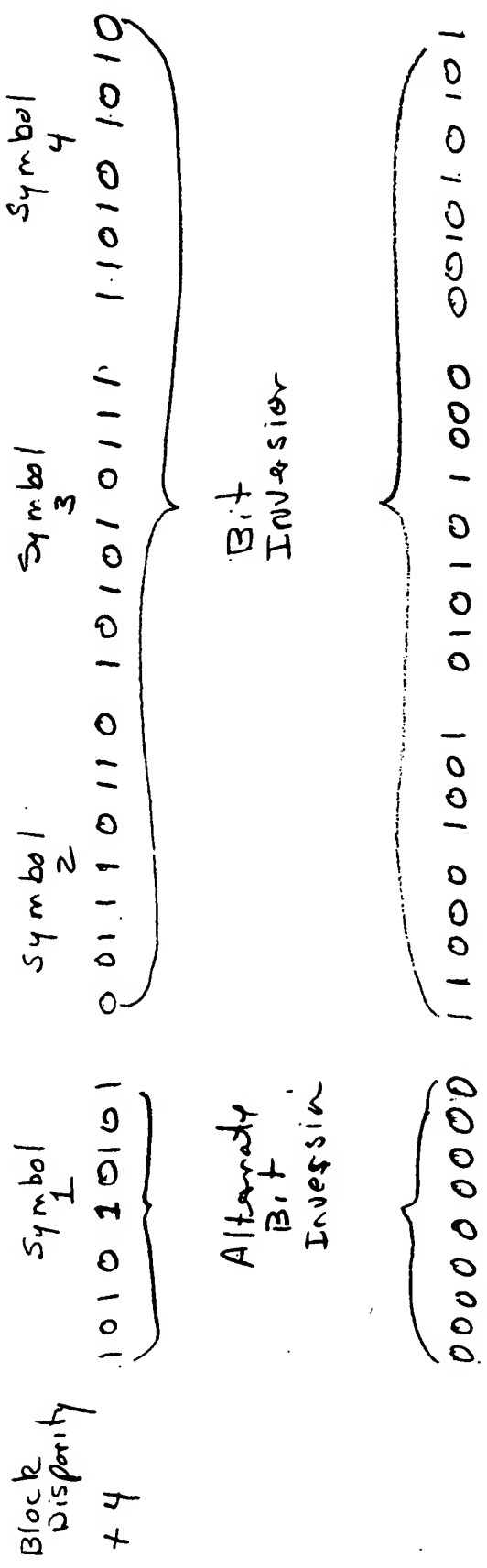


Fig 21A

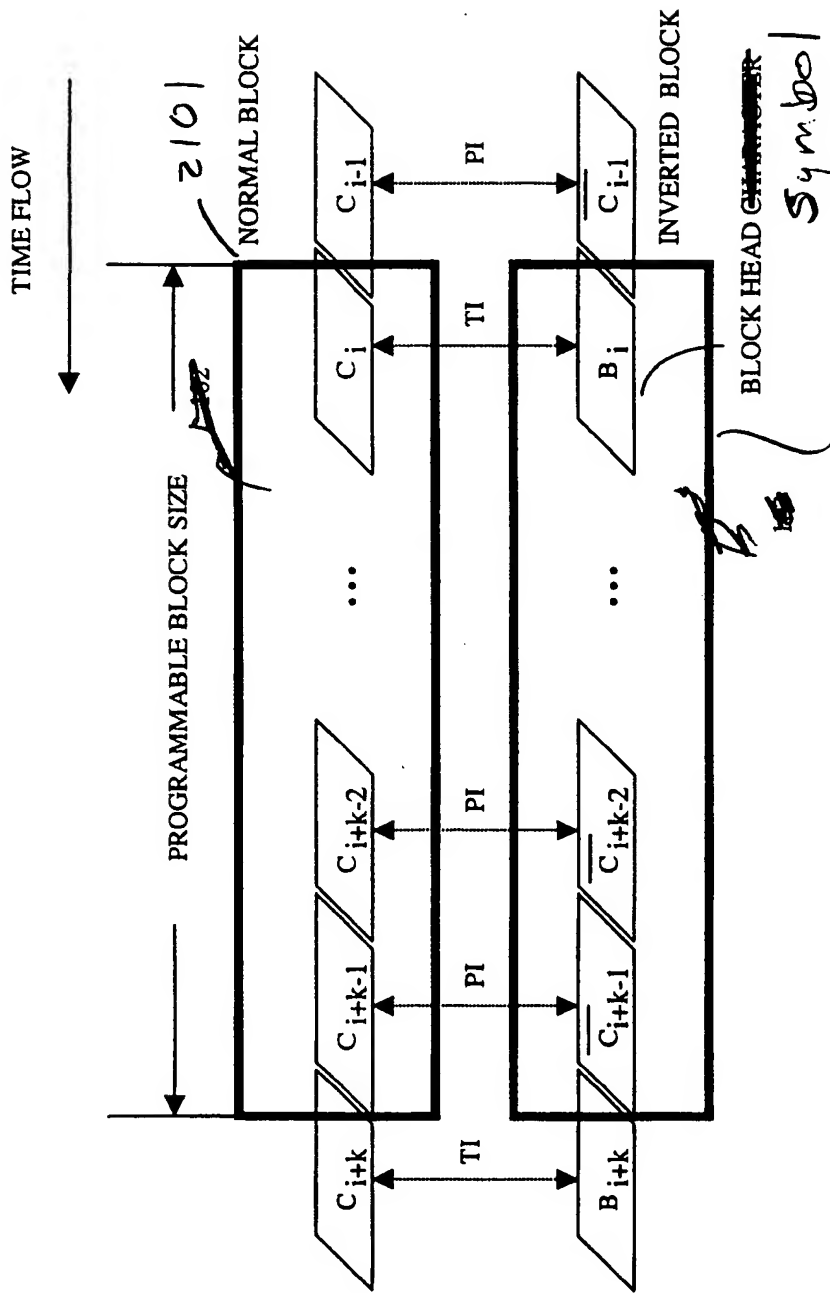


Fig 21B

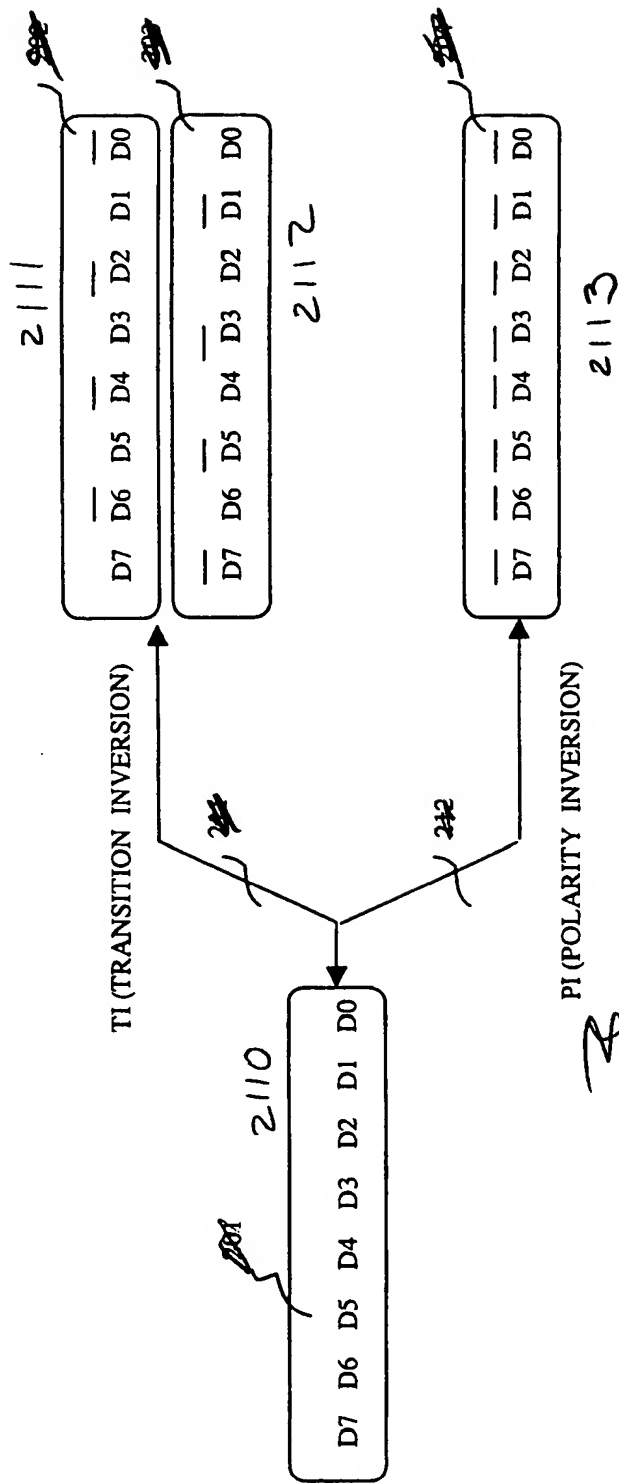


Fig 21C

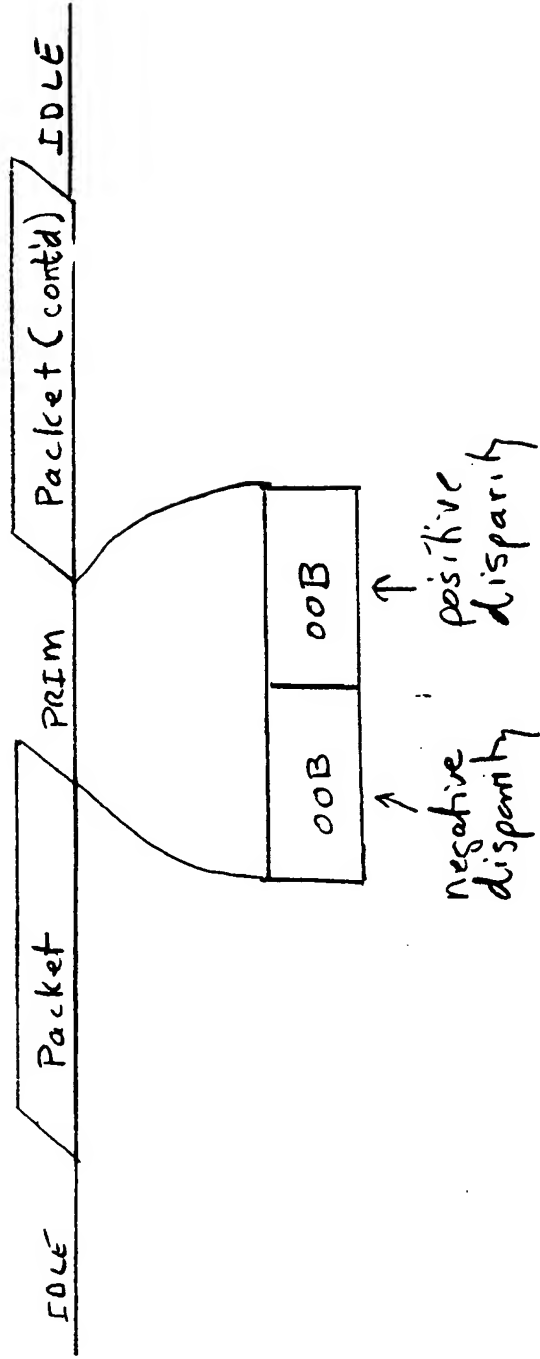


Fig 22

10053461.110701

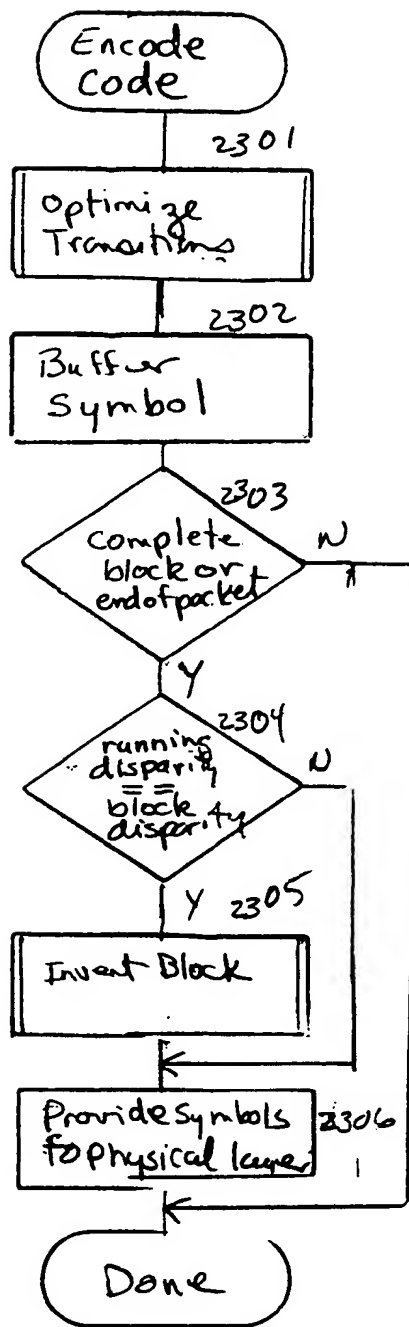


Fig 23

Optimize
Transitions

2401

receive
code

2402

count
transitions

2403
number
of transitions
≤ 4

N

2404

set 9th bit
to 0

Y 2405

invert every
other bit

2406

set 9th bit
to 1

2407

symbol is
9th bit + code

Done

Fig 24

Invert
Block

2501

select 1st
symbol of group

2502

inverts every
other bit

2503

select next
symbol of
block

2504

all symbols
already
selected

y

Done

N2505

invert bit of
selected symbol

Fig 25

10053461.110701

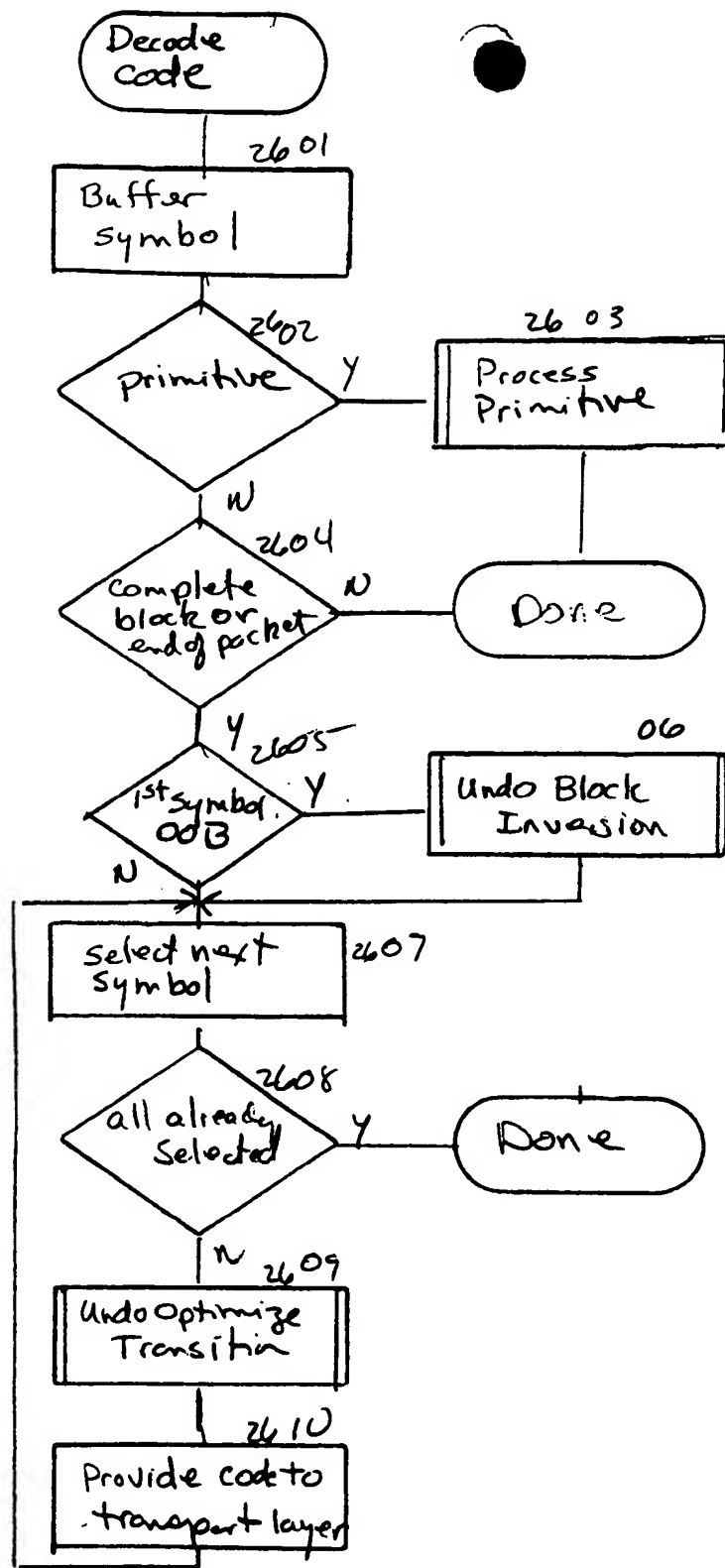


Fig 26

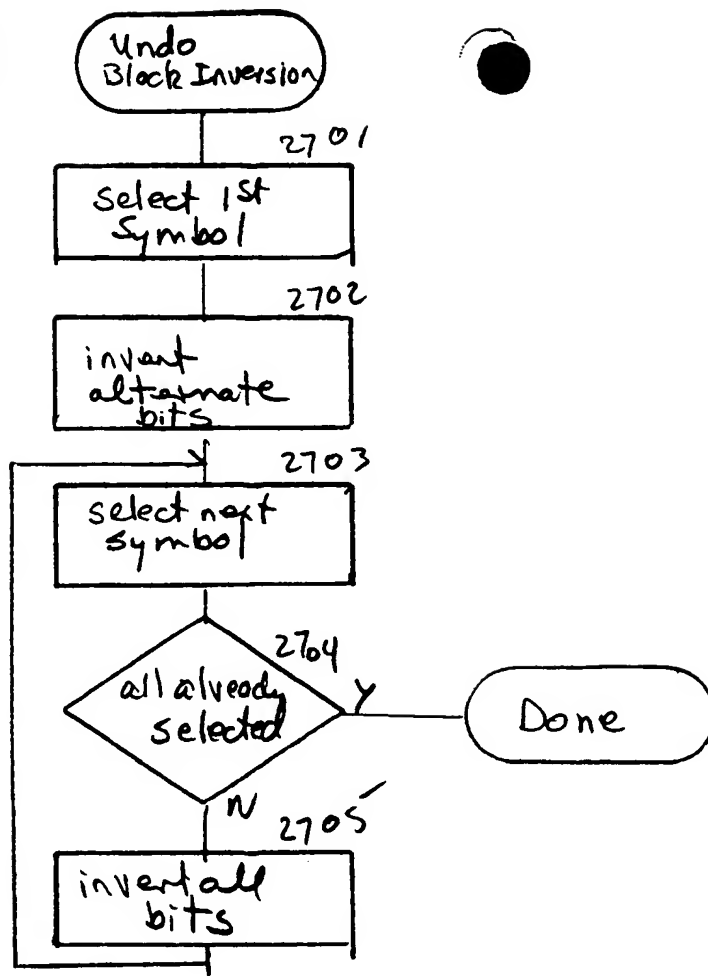


Fig 27

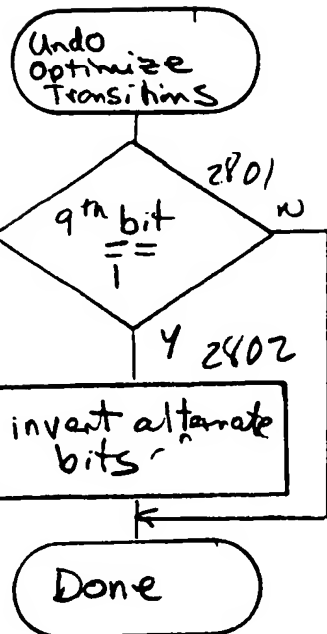


Fig 28

10053461.10701

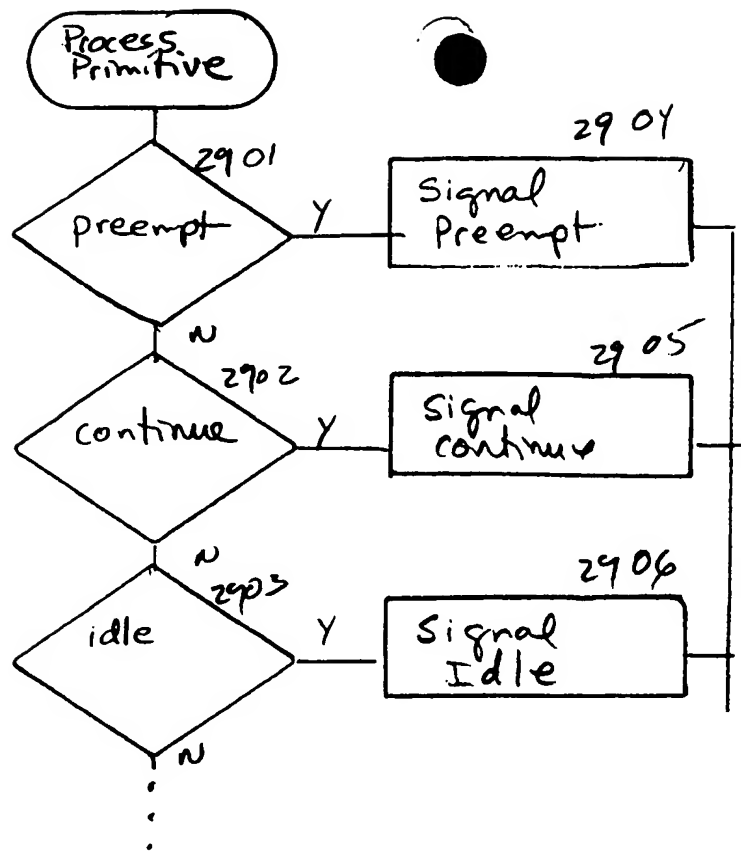


Fig 29

Multipoint Memory Device 3000

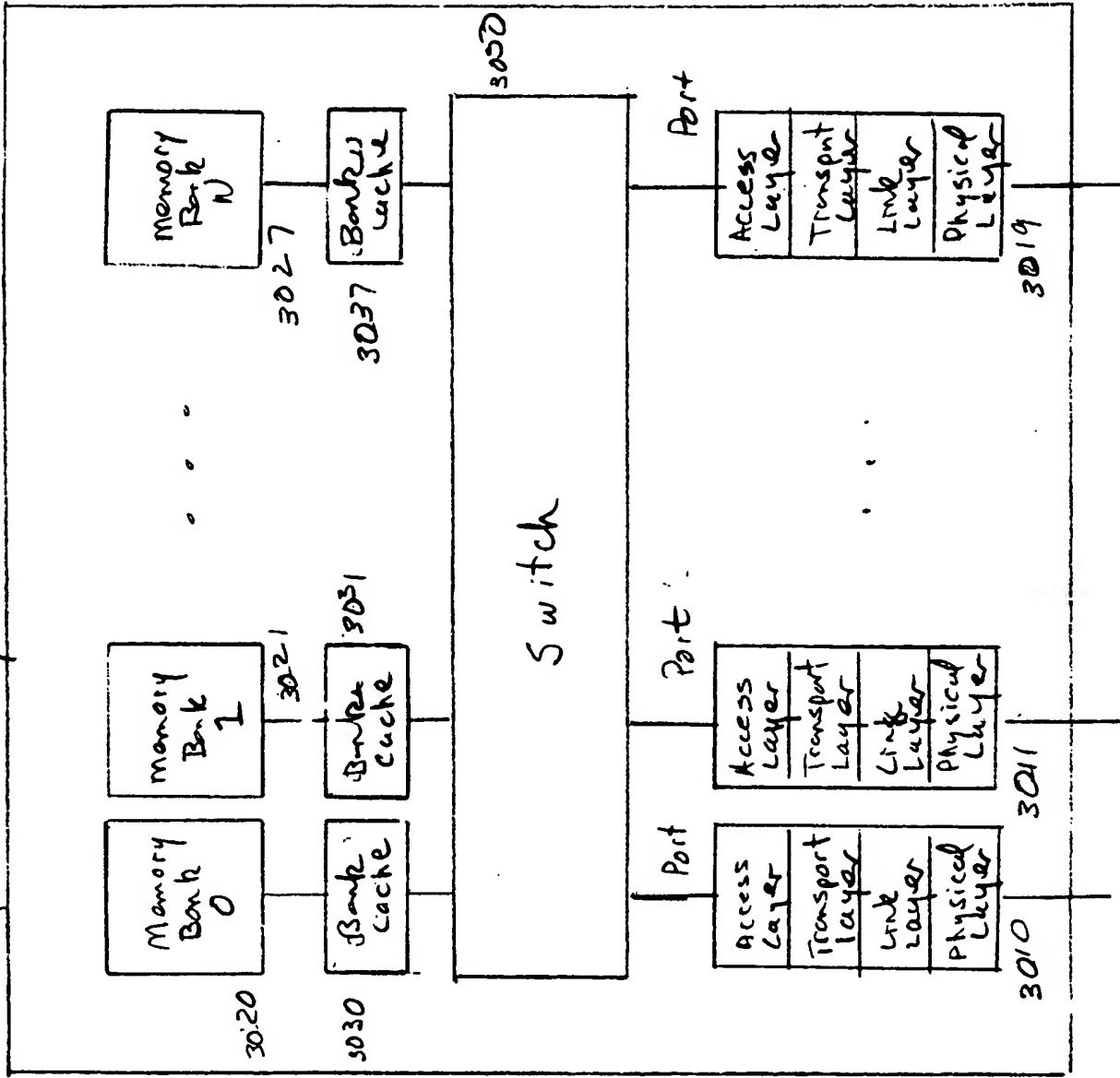
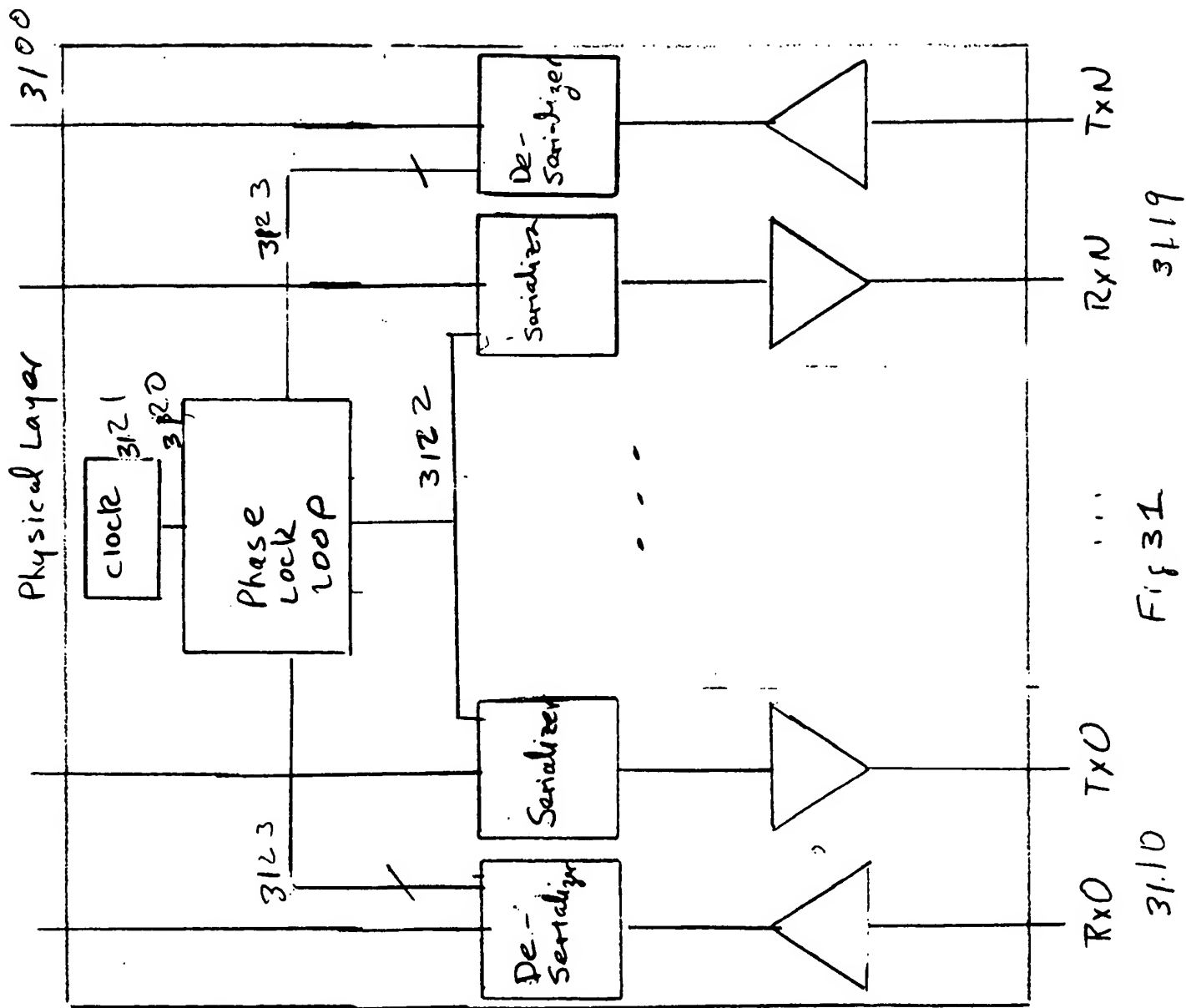


Fig 30



Input Queue 3201				Output Queue 3202			
Port	R/W	Address	Data	Valid	Port	Data	
3	R	1000		1	3	11...0	
4	W	4000	10...1	0			
3	W	1000	111...0	0			
3	R	2000		1	3	101...1	
					⋮		

Fig 32

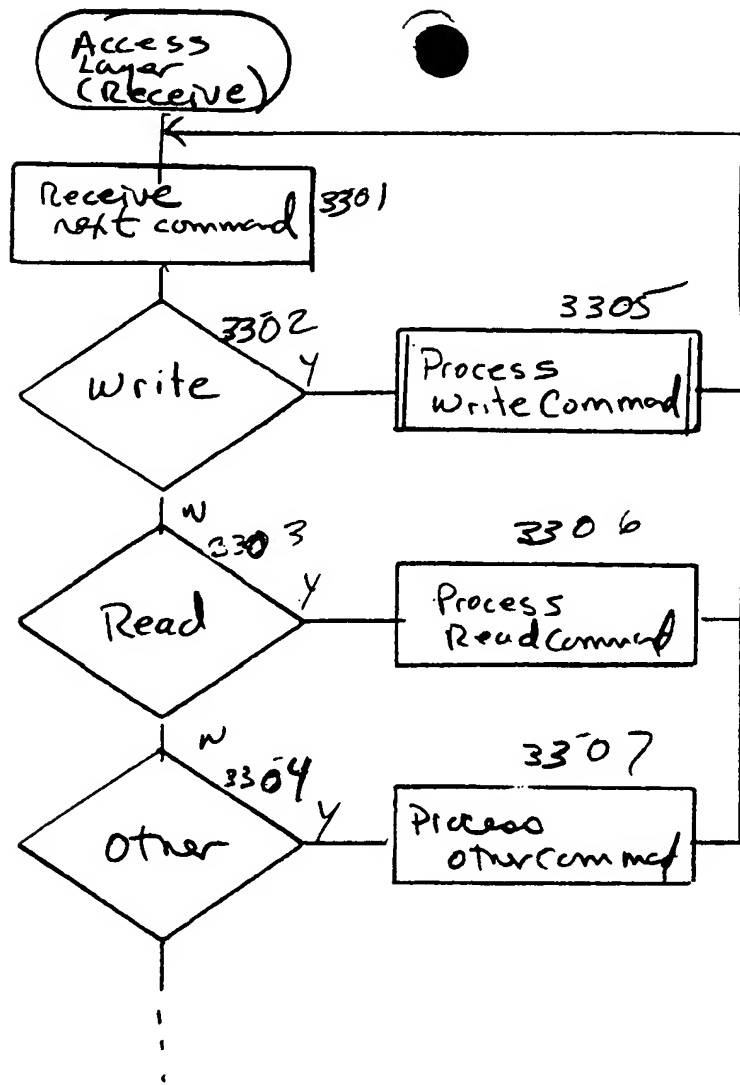


Fig 33

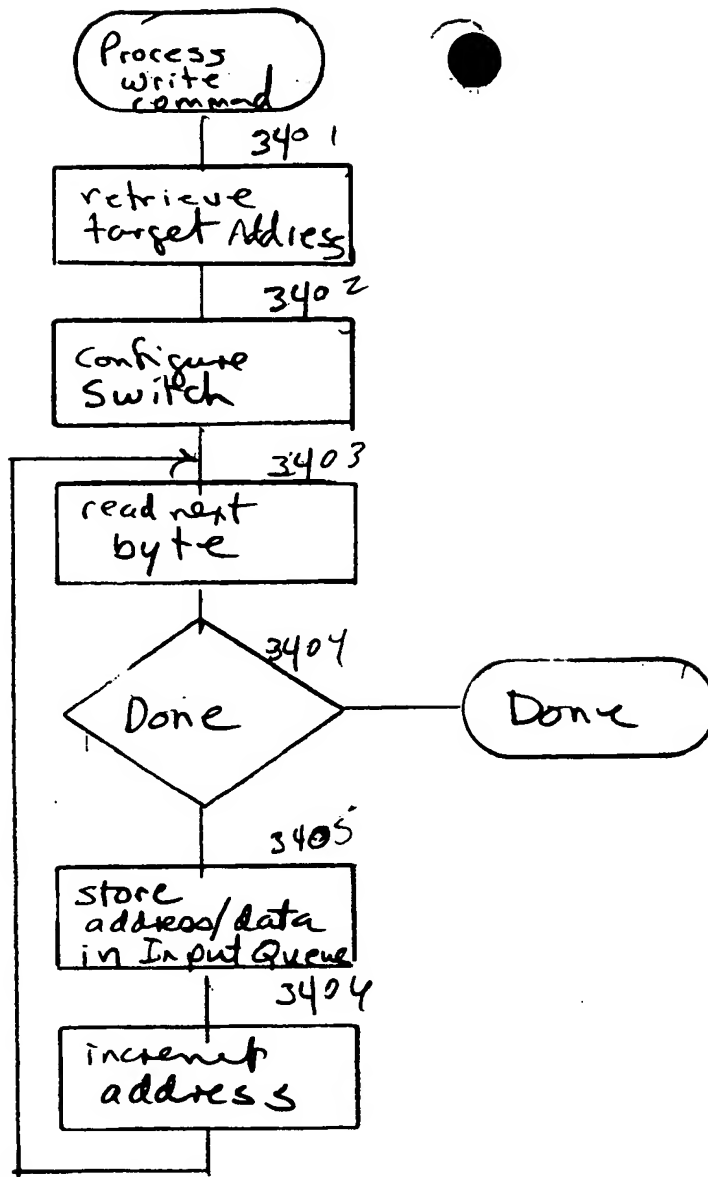


Fig 34

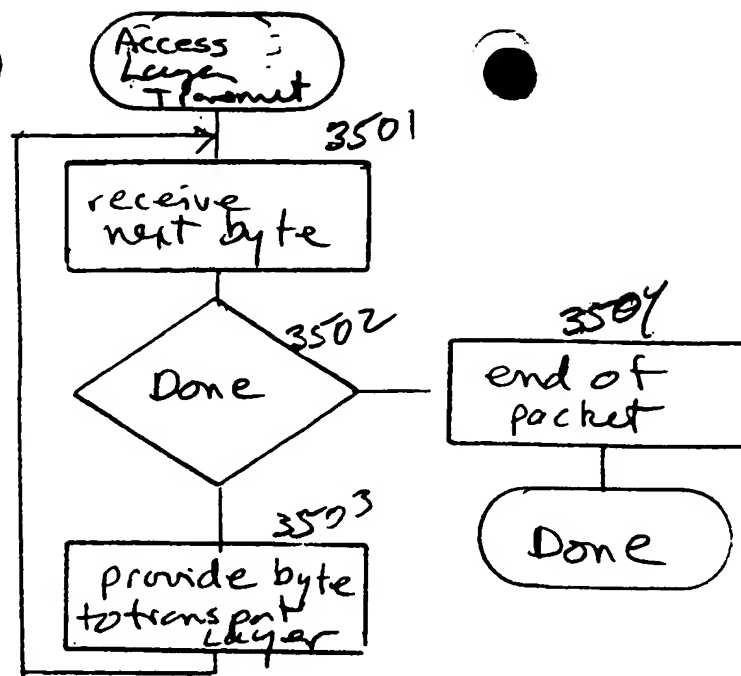
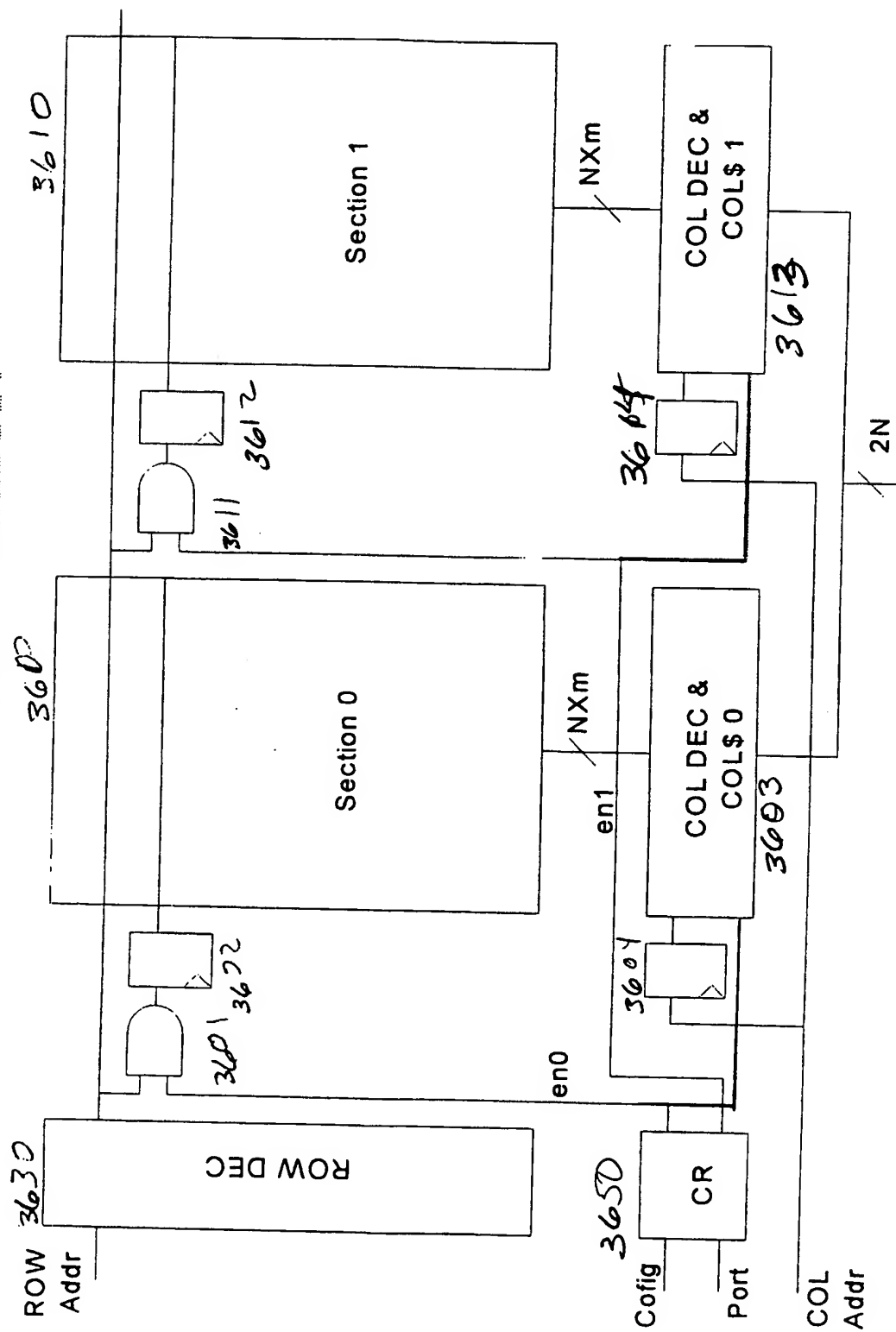
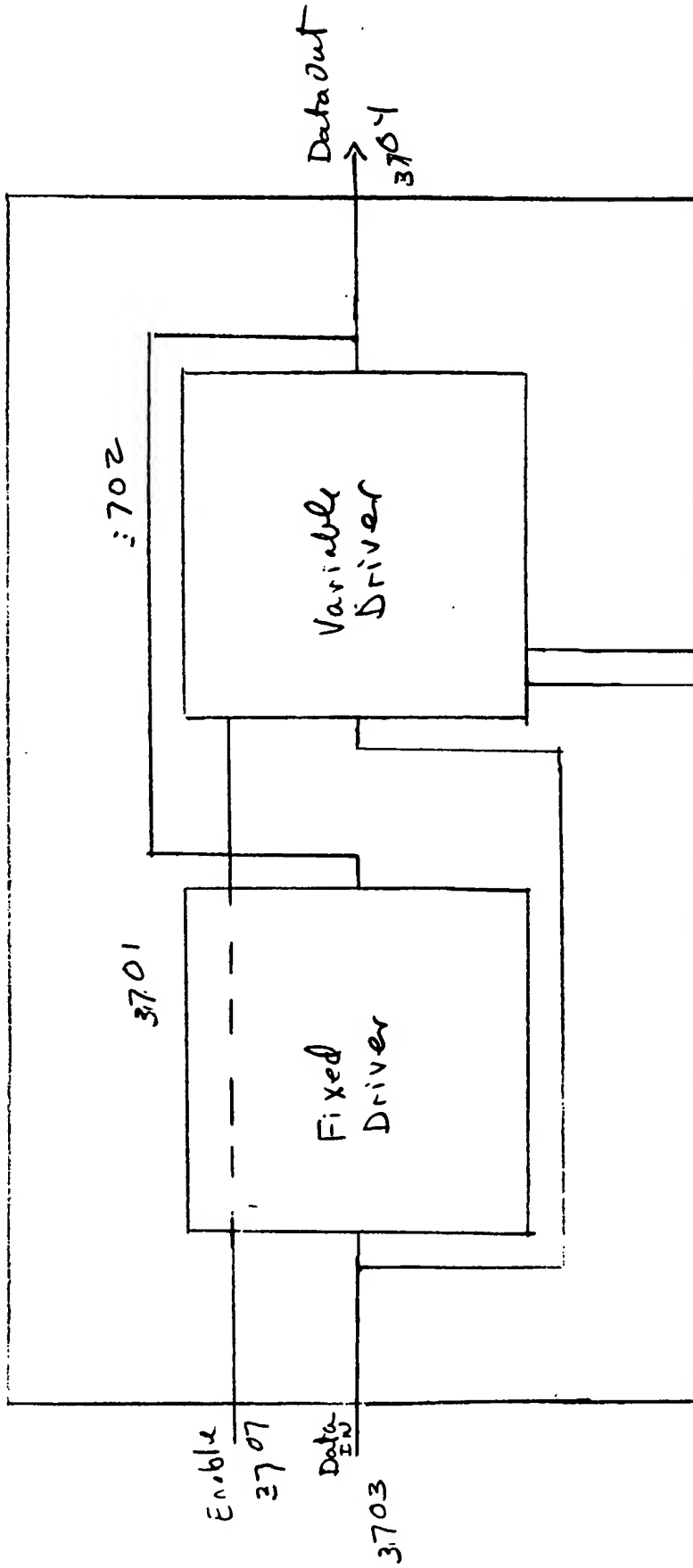


Fig 35

[illegible]

Li³⁺

Line Driver 3700



RD⁺ 3705
RD⁻ 3706

Variable Driver
 $\begin{cases} RD^+ \wedge \overline{DataIn} = \text{pull down} \\ RD^- \wedge DataIn = \text{pull up} \end{cases}$

Fig 37A

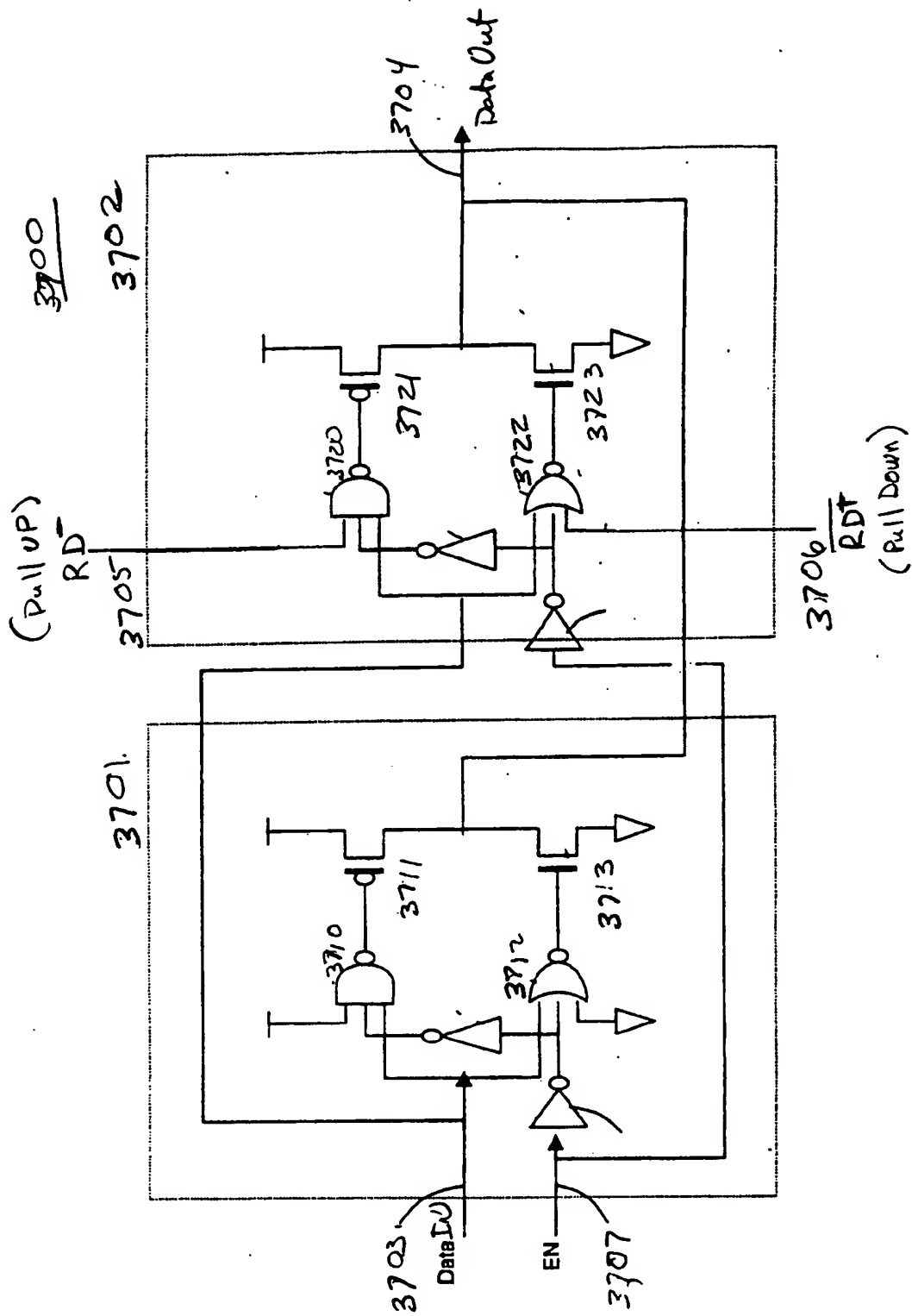


Fig 37B

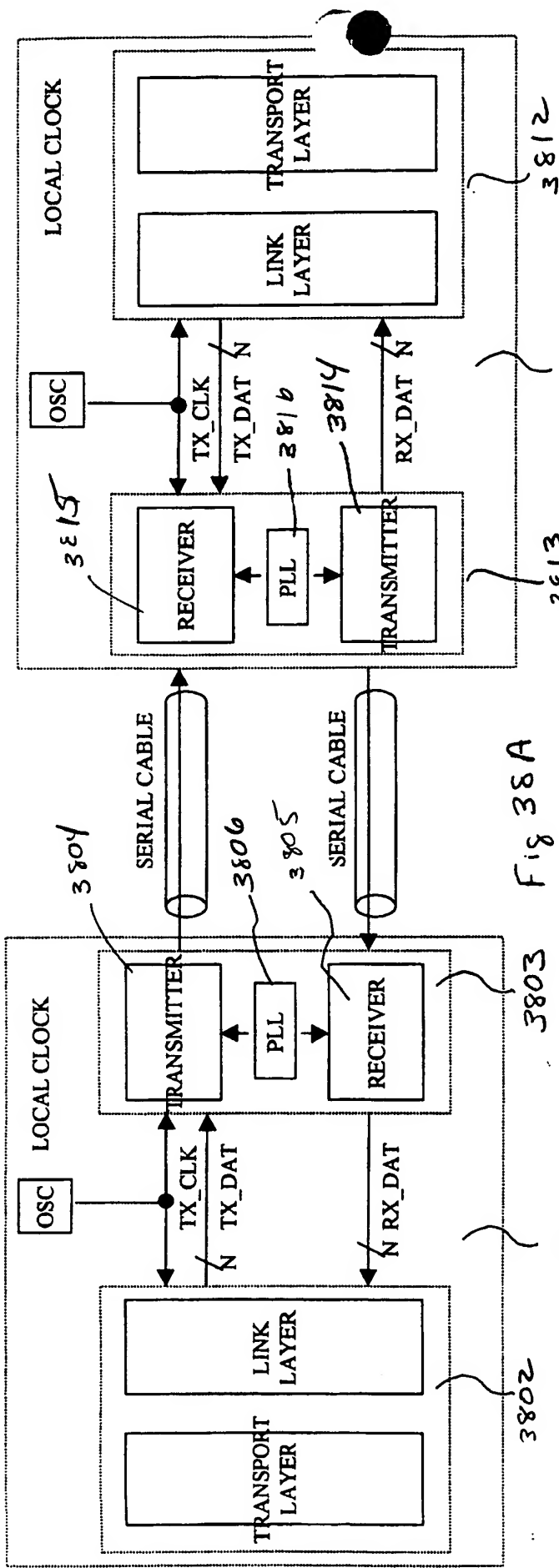


Fig 38A

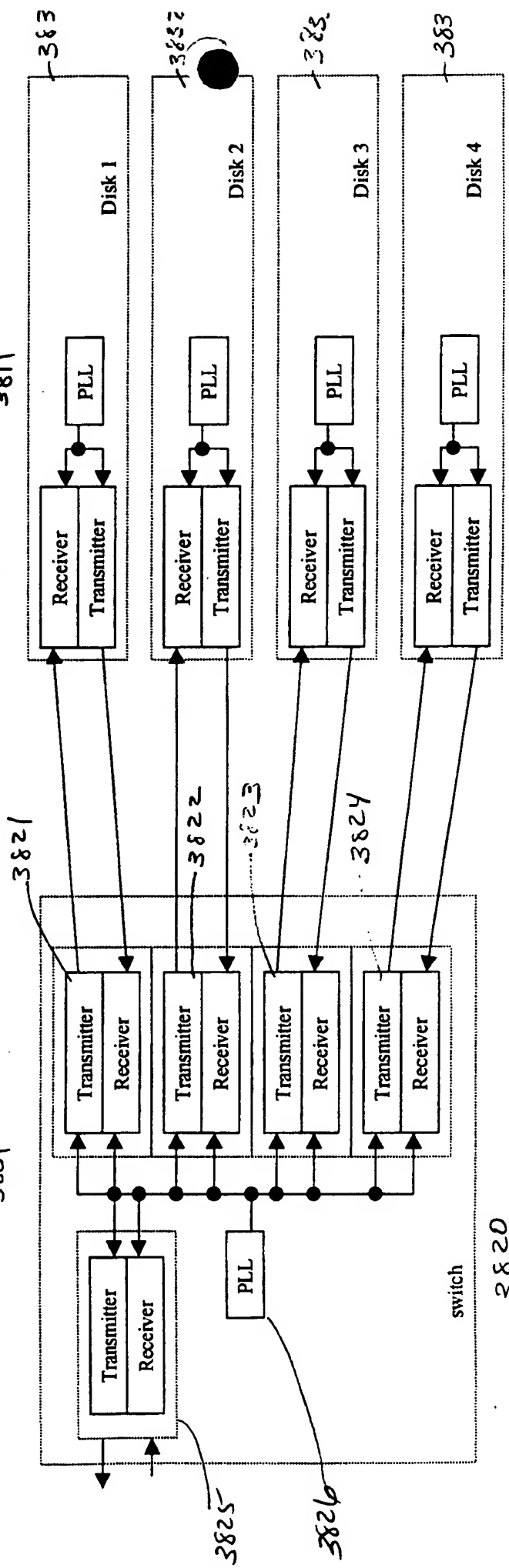


Fig 38B

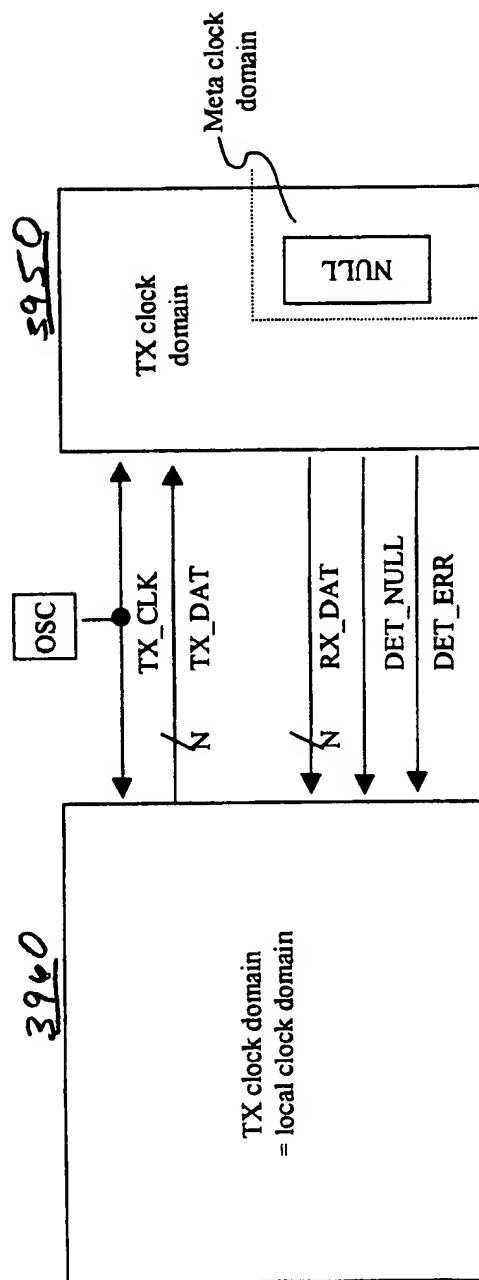
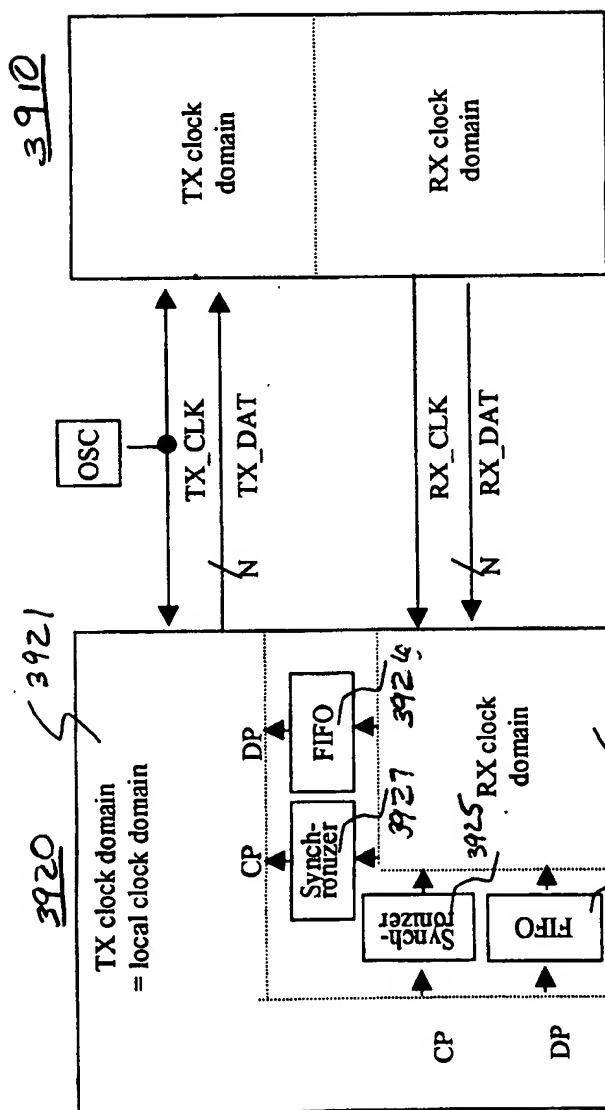


FIG. 40

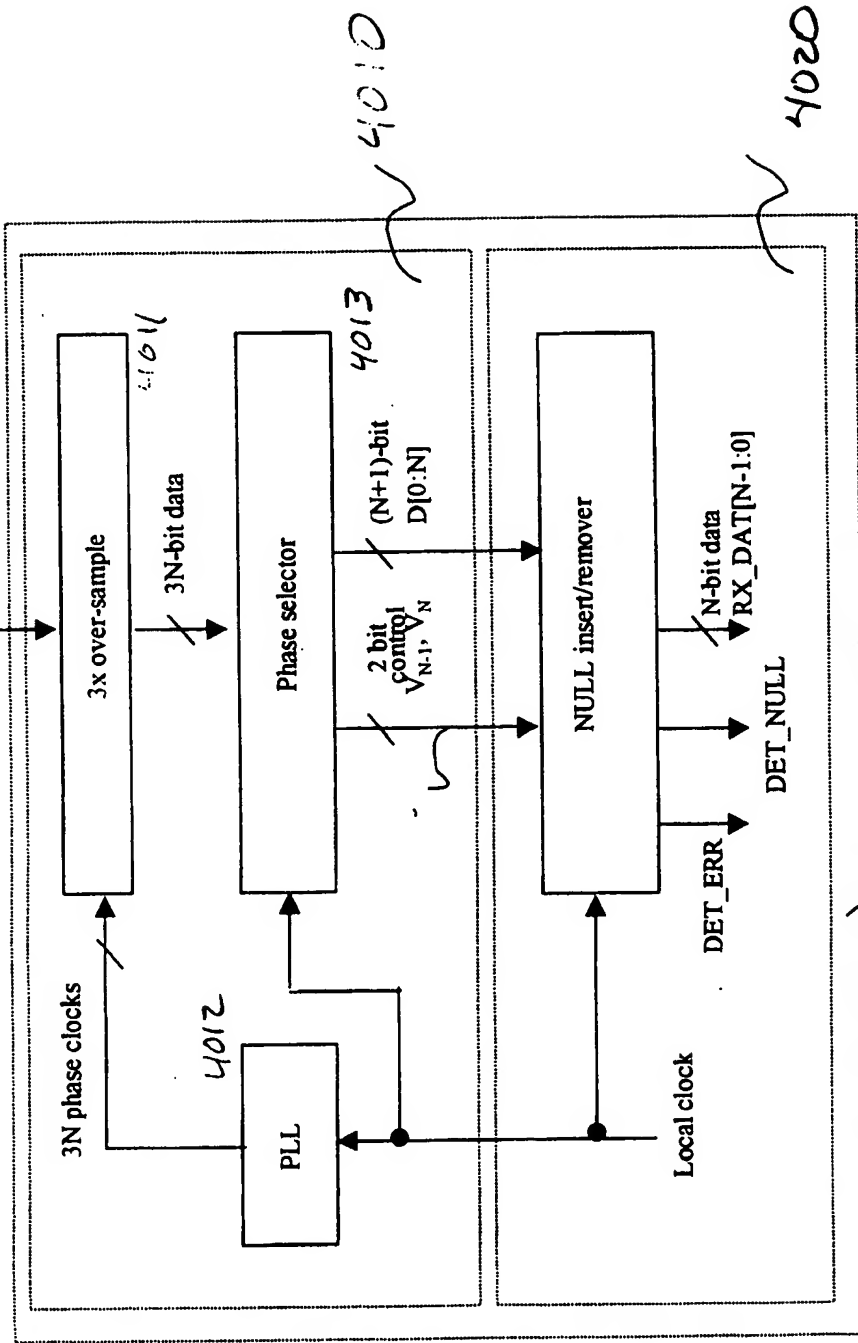


Fig 40

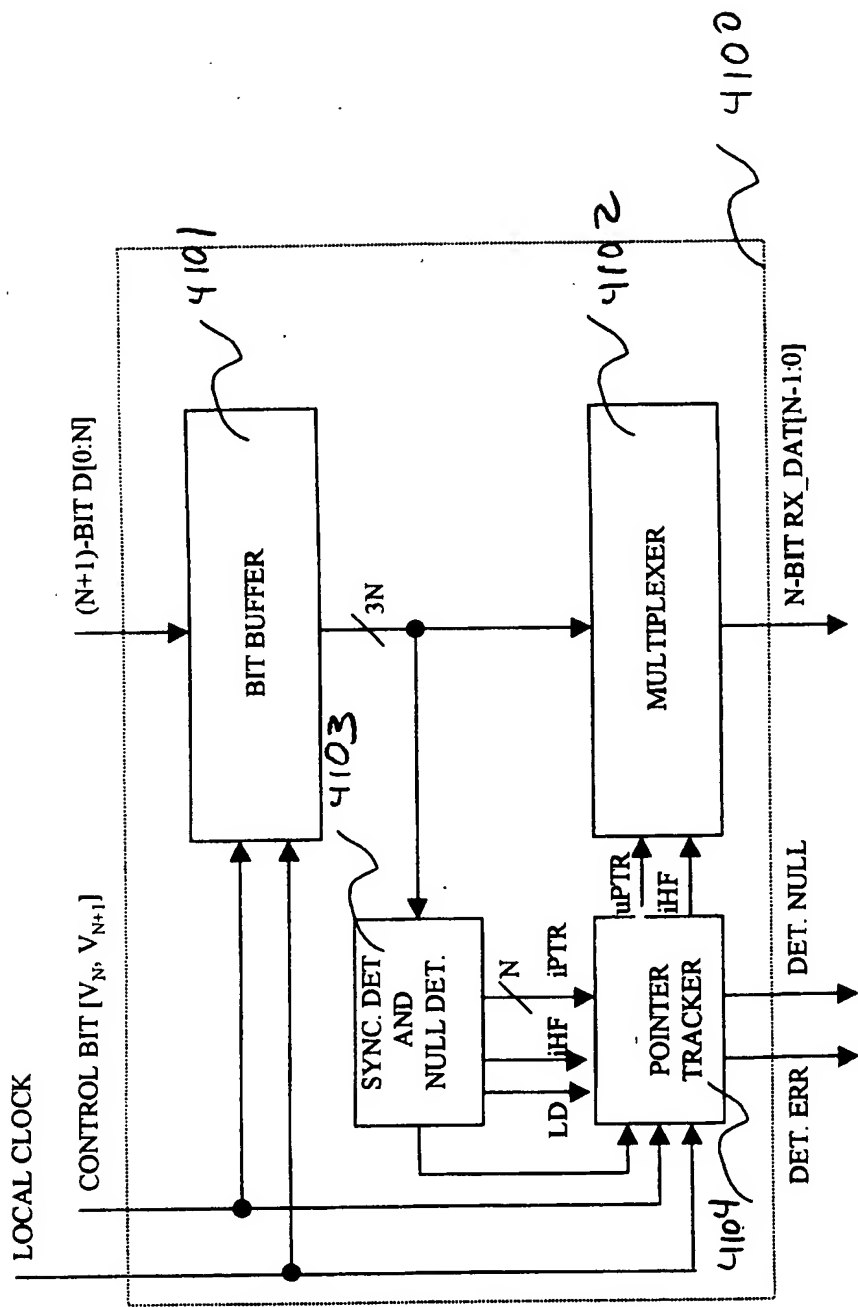


Fig 41

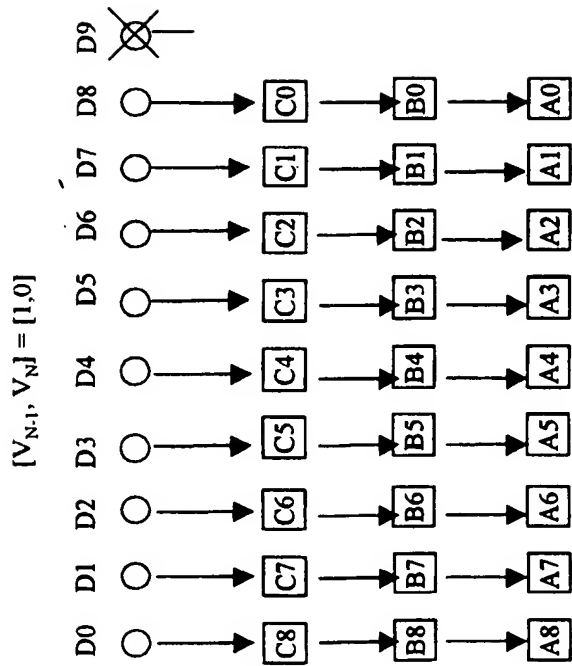


Fig 42A

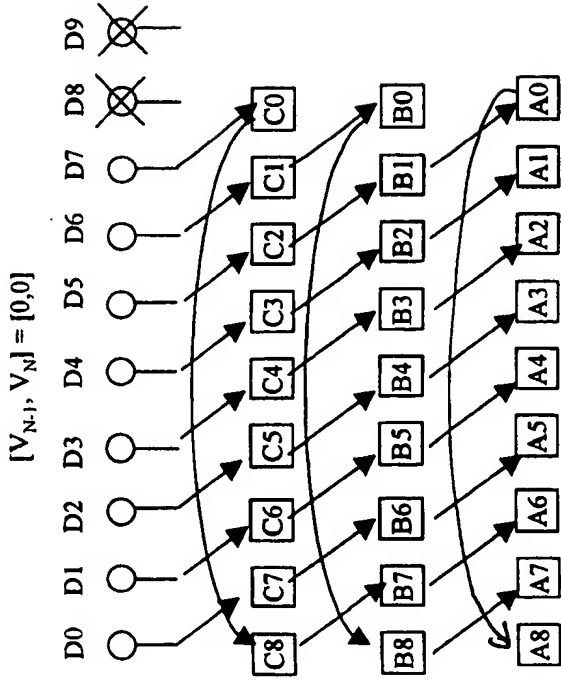


Fig 42B

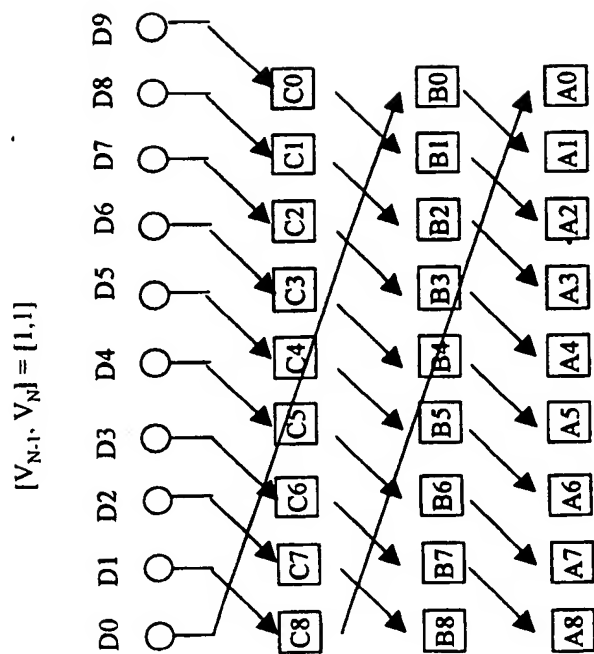


Fig 42c

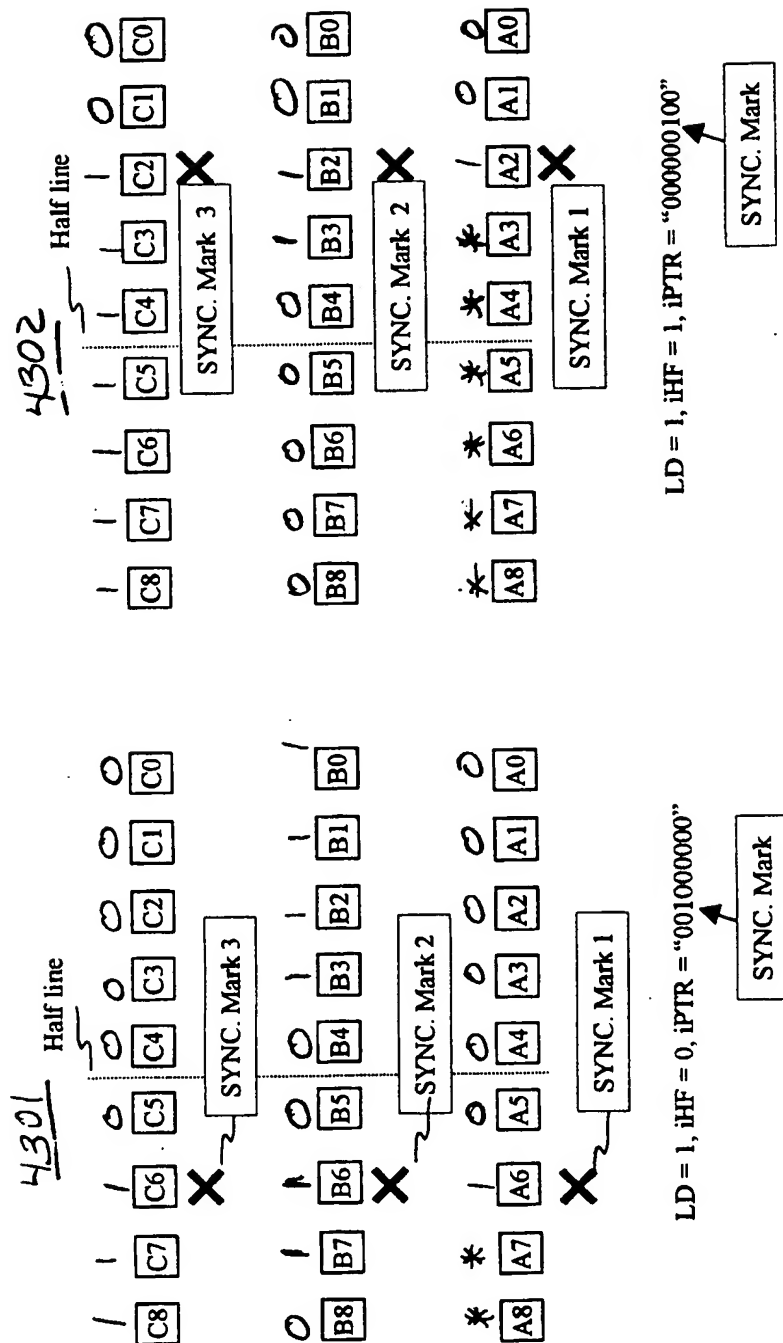
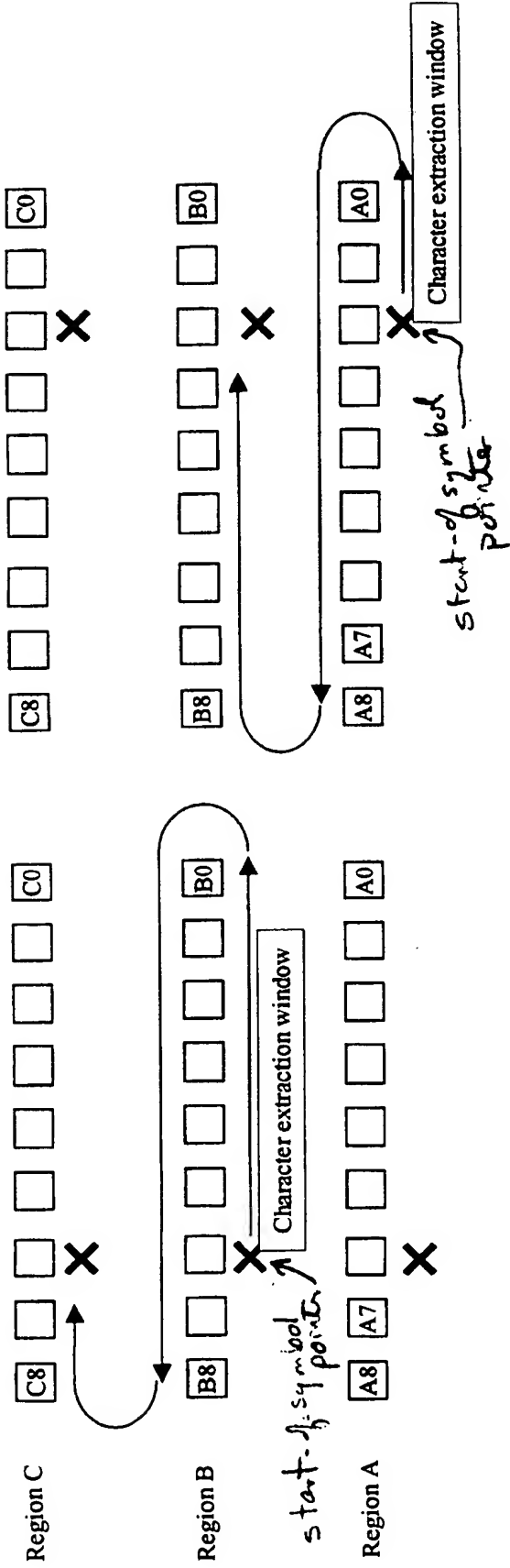


Fig. 43



LD = 1, iHF = 0, iPTR = "001000000"

LD = 1, iHF = 1, iPTR = "000000100"

Fig 44

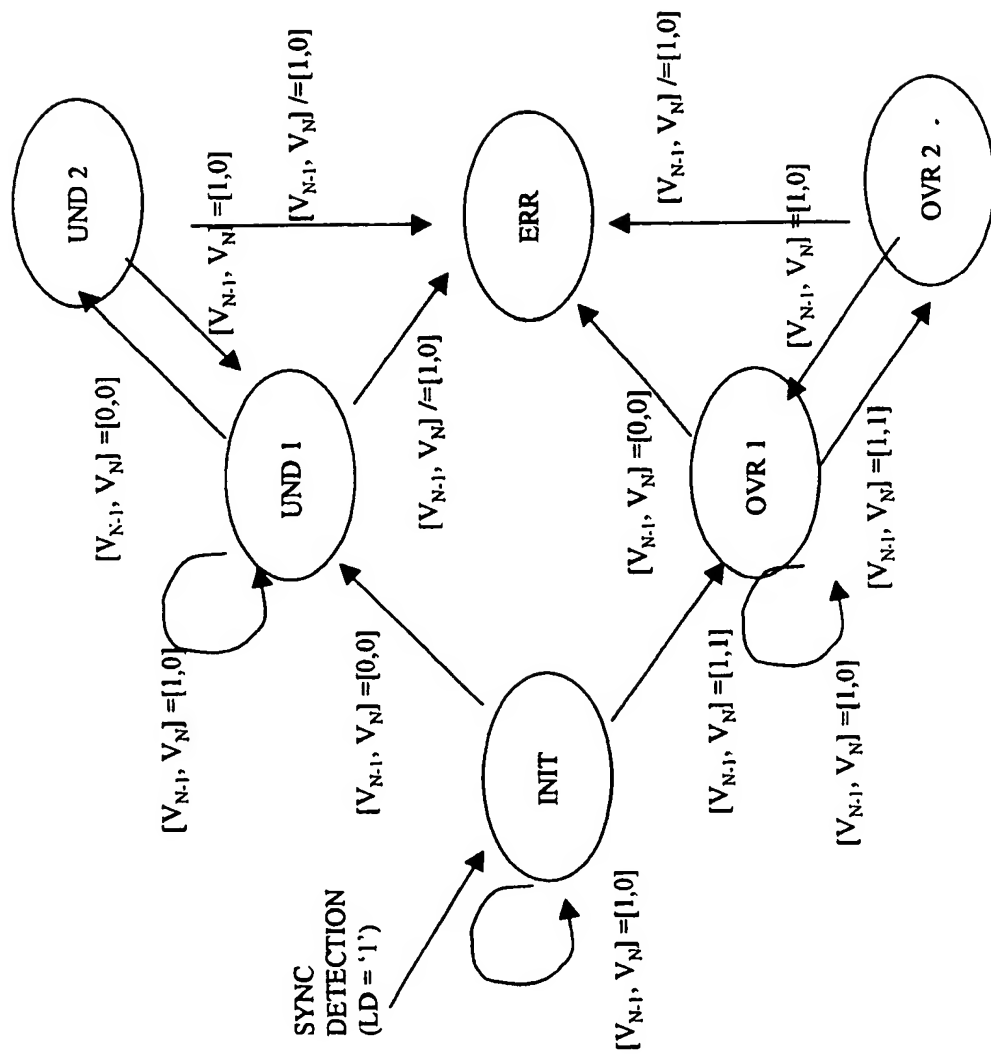


Fig 45

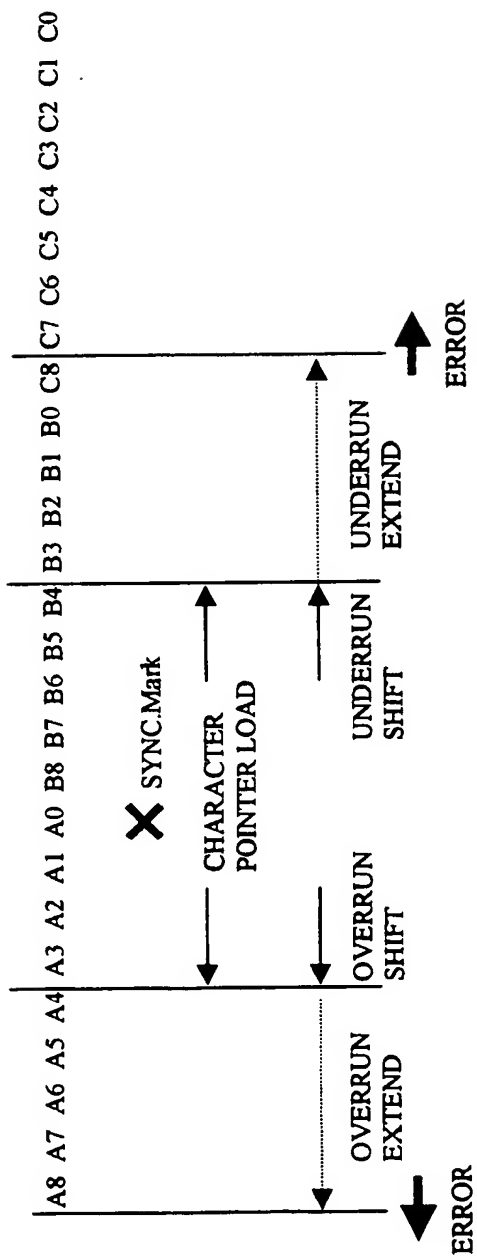


Fig 46

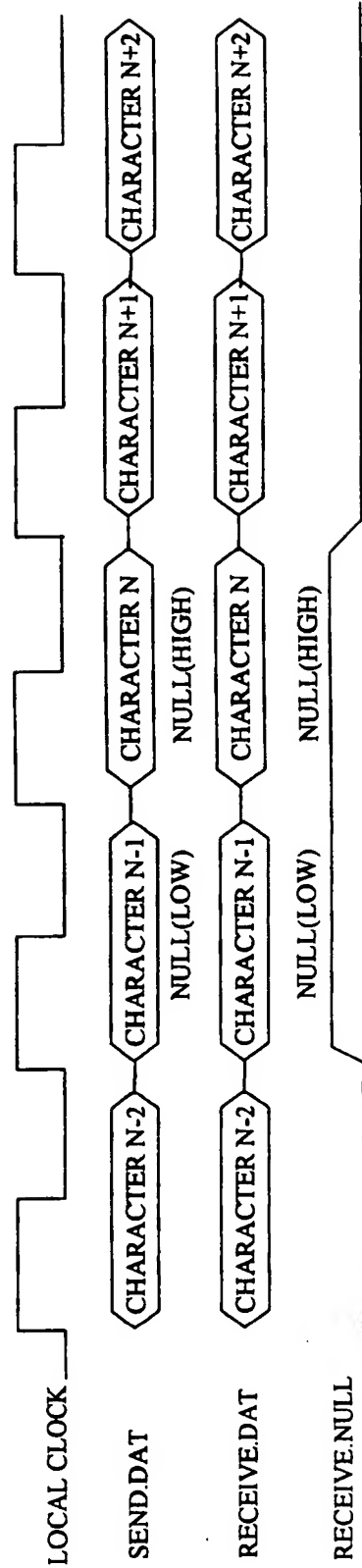
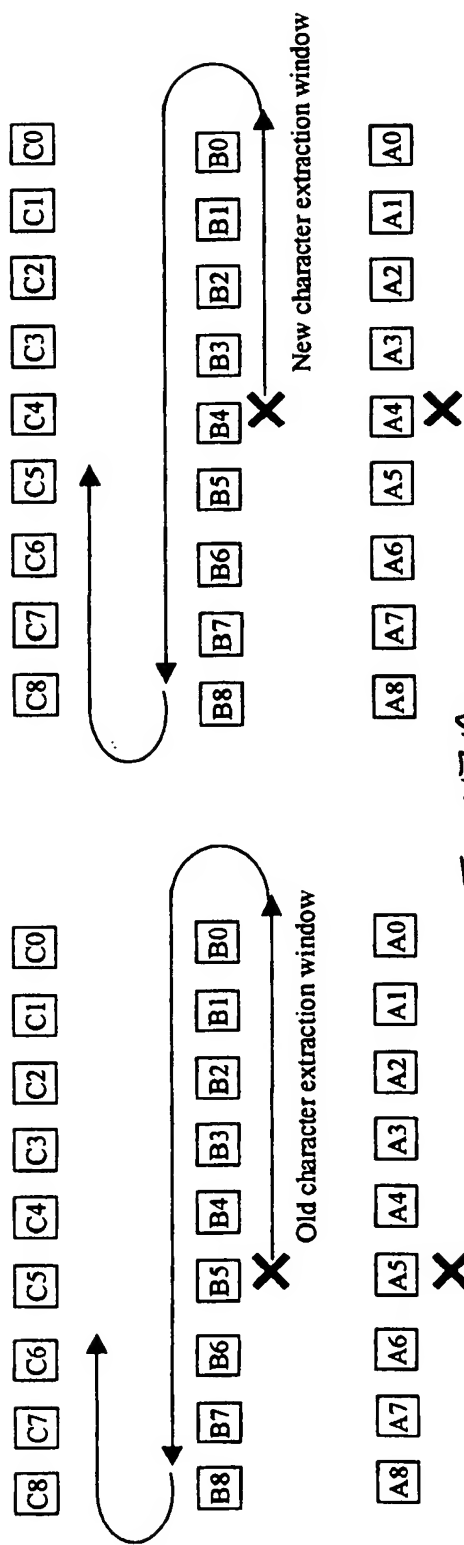


FIG 47B

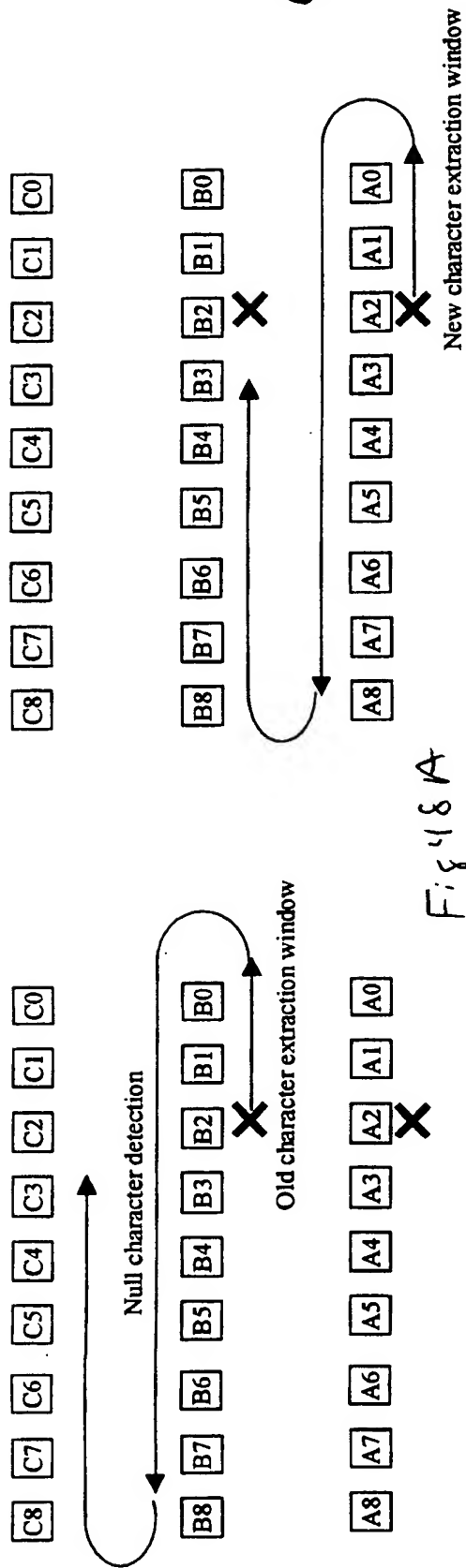


Fig 48A

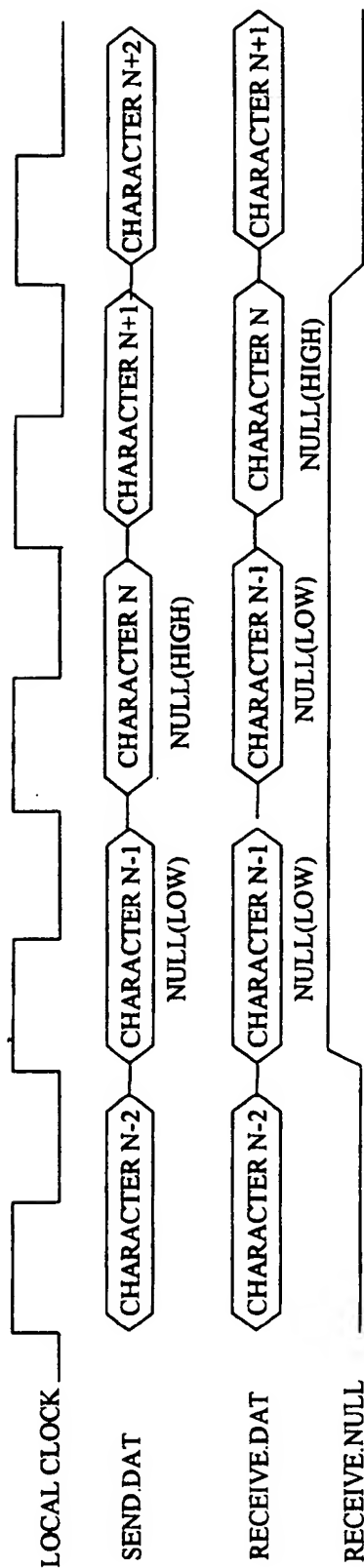


Fig 48B

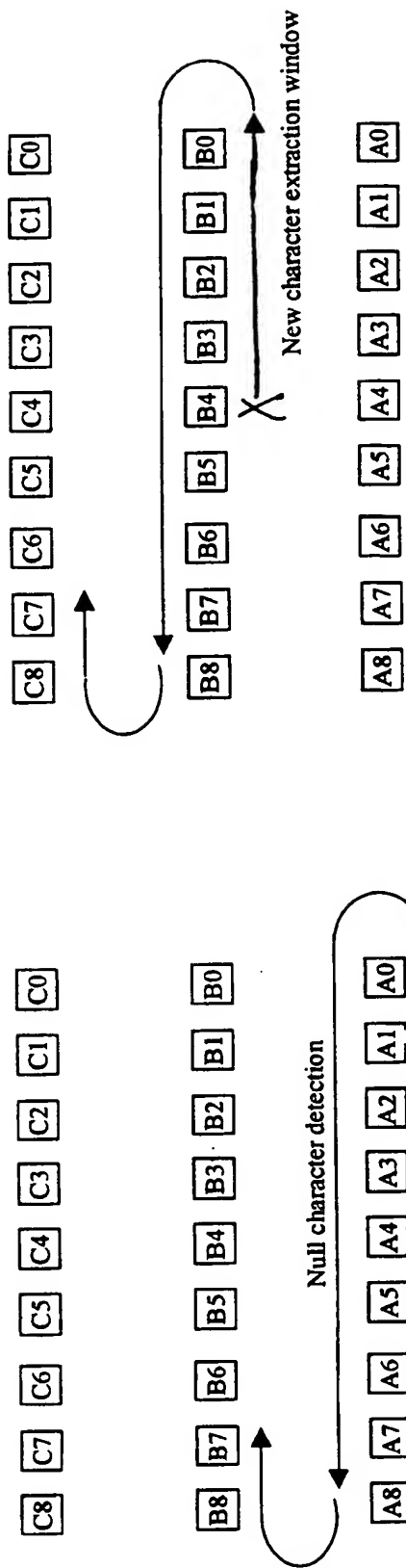


Fig. 49A

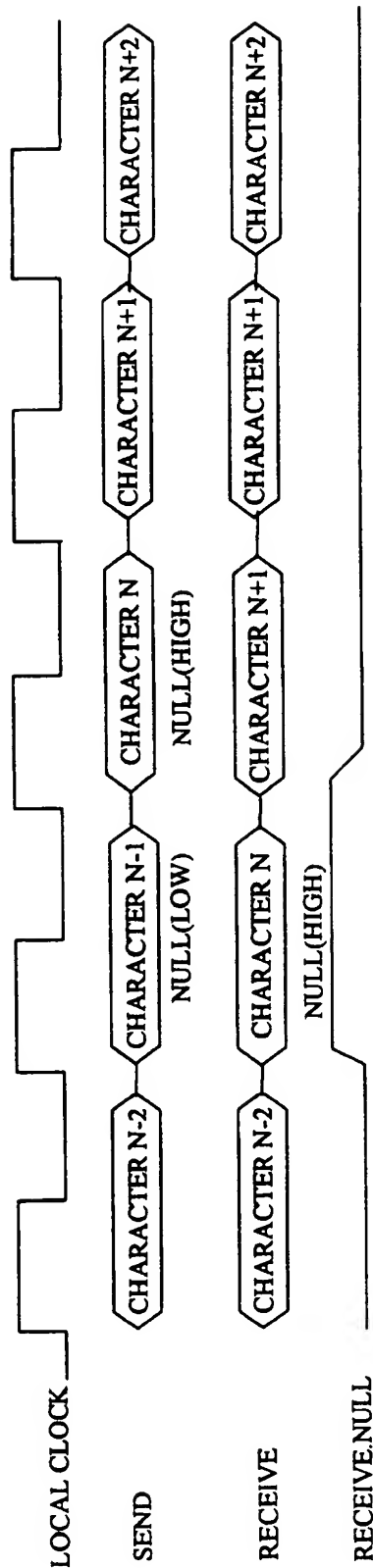


Fig. 49B